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U.S. DEPARTMENT OF COMMERCE/National Bureau of Standards

Semiconductor Measurement Technology:

NBS/DOE Workshop, Stability of (Thin Film) Solar Cells and Materials

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PREFACE

The Workshop on Stability of (Thin Film) Solar Cells and Materials was conducted as part of the Semiconductor Technology Program in the Electron Devices Division of the National Bureau of Standards (NBS).

The Semiconductor Technology Program serves to focus NBS efforts to enhance the performance, interchangeability, and reliability of discrete semiconductor devices and integrated circuits through improvements in measurement technology for use in specifying materials in national and international commerce and for use by industry in controlling device fabrication processes. Its major thrusts are the development of carefully and well-documented test procedures and associated technology and the dissemination of such information to the electronics community. Application of the output by industry will contribute to higher yields, lower cost, and higher reliability of semiconductor devices. The output provides a common basis for the purchase specifications of government agencies which will lead to greater economy in government procurement. In addition, improved measurement technology will provide a basis for controlled improvements in fabrication processes and in essential device characteristics.

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Semiconductor Measurement Technology:
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David E. Sawyer and Harry A. Schafft
Editors

A workshop was held to discuss what needs to be done to achieve and measure long term stability of terrestrial solar cells using thin film materials and device technologies. Under this theme, researchers in the field and invited speakers from related device technologies presented papers and took part in discussions related to solar cells of the following three material groupings: (1) Cu_2S/[CdZn]S, Cu-ternaries/CdS, InP/CdS, and amorphous Si; (2) polycrystalline, metal-insulator-semiconductor (MIS), and conducting-oxide Si; and (3) polycrystalline and antireflection-coated metal-oxide-semiconductor (AMOS) GaAs. This workshop report contains the 18 papers presented and the reports of three discussion groups; it also includes a section on the highlights of these papers and reports. The many needs identified by the workshop participants can be organized into two general areas of work to be done. One area of work is in the development of an improved understanding of cell operation and of component structures of these cells. The other is in the development of an improved measurements base.

Key Words: Accelerated tests; failure mechanisms; failure modes; photovoltaics; reliability; semiconductors; solar cells; stability; testing; thin films.

1. INTRODUCTION

A Workshop on the Stability of (Thin Film) Solar Cells and Materials was conducted by the National Bureau of Standards at its Gaithersburg, Maryland, site on May 1 to 3, 1978, for the Department of Energy's Advanced Materials Research and Development Branch in support of the Department's National Photovoltaic Program. The purpose of the workshop was to identify obstacles to achieve stability and long life of terrestrial solar cells developed using thin film material and advanced device technologies. An important part of the workshop was to discuss and suggest how these obstacles could be overcome by the development and use of test and measurement procedures designed to enhance the prediction of material and device stability.

Three groups of exploratory solar cell materials and device concepts were considered at the workshop: (1) Cu_2S/[CdZn]S, Cu-ternaries/CdS, InP/CdS, and amorphous Si; (2) polycrystalline, metal-insulator-semiconductor (MIS), and conducting-oxide Si; and (3) polycrystalline and antireflection-coated metal-oxide-semiconductor (AMOS) GaAs. Researchers in these technologies, joined by invited measurement experts in related technical areas, convened to address the issues of the workshop. In all, 102 scientists and engineers took part in this effort.

The workshop was divided into three sessions. In the first, researchers reviewed modes and mechanisms for degradation and failure and the status of present reliability testing, pertinent to the three groupings. In the second session, speakers from related device technologies discussed measurement and test approaches that they have used for achieving high reliability in their device areas. Three discussion groups were formed for the third session, one for each of the three cell and material classifications. The task of these groups was to identify what means are available and what is to be done to satisfy needs in achieving goals for long term stability of advanced-technology solar cells. Reports of these working groups were presented by the group chairmen at the final session of the workshop.

To serve as summary, the next section provides the highlights of the presentations and discussion group reports. The title and author(s) of each presentation are located in the margin adjacent to the highlight. Following these highlights are two brief introductory statements: one by D. L. Feucht about the Department of Energy's (DOE's) program on the development of thin film solar cells in the context of the National Photovoltaic Program, and one by L. M. Magid about DOE's plans to develop a standards base for photovoltaic systems. This report is completed with the papers submitted by the speakers and discussion group leaders, arranged by session.

A separate report[1] has been prepared which is intended to supplement this formal workshop report. It considers the results of the workshop from the perspective of measurement requirements related to the achievement of cell stability and reliability. This separate report integrates the recommendations made and needs identified by the participants of the workshop in the context of this perspective. The result of this integration is the conclusion that there are serious deficiencies in the ability to make meaningful estimates of long term cell stability and in the ability to make knowledgeable decisions about material, device, and process design improvements. These deficiencies stand in the way of achieving the performance goals for efficiency and long term stability of the thin film solar cell program. Two general areas of work are identified where increased efforts are required. One general area is in the development of a better understanding of the operating principles of these cells; of material, processing, and assembling factors that affect cell performance; and of cell degradation mechanisms. The other general area is in the development of not only test methods and procedures for testing materials and cells, but the development, as well, of requirements for reporting material and cell test data.

2. HIGHLIGHTS OF WORKSHOP SESSIONS

Session I: Status of Present Reliability Testing, Failure Modes, Failure Mechanisms, and Data for Thin Film Solar Cells and Materials

The Stability & Reliability of CdS/Cu_2S Solar Cells, J. D. Meakin and J. E. Phillips, Univ. of Delaware

The primary degradation mechanisms of the Cu_2S/CdS heterojunction cell are the oxidation of Cu_2S, diffusion of Cu into CdS, electrolytic decomposition of Cu_2S to nucleate copper, and loss of structural integrity of electrical contacts and device/encapsulant interfaces due to thermal expansion mismatch and UV-induced bond strength degradation, respectively.

None of these degradation mechanisms preclude 10- to 20-year life, but the measurement of the rate of degradation of these cells and hence the prediction of life is a problem. To use accelerated test procedures to predict life requires a detailed knowledge of the mechanisms being accelerated. For thin film solar cells in general and for Cu_2S/CdS cells in particular, this information is not available. Meaningful accelerated testing will not be possible until accelerated tests are matched to specific degradation mechanisms in a knowledgeable way.

The following four major research needs for Cu_2S/CdS solar cells were identified: (1) Work is needed to improve and define the quality of the cell's hermetic protection, because these cells will degrade rapidly if exposed to air. This effort should also include the development of a quantitative understanding of the oxidation of the Cu_2S layer and the resultant structural and electronic changes. (2) The interdiffusion mechanisms which reduce cell performance need to be identified. (3) The relation of various structurally related degradation modes, such as encapsulation

[1] Schafft, H. A., and Sawyer, D. E., A Perspective of a Workshop on Stability of (Thin Film) Solar Cells and Materials, NBSIR 79-1778, June 1979.

delamination and loss of grid contact, to use-conditions needs to be identified. And, (4) the relationship between copper nodule formation (due to electrolytic decomposition of Cu_2S) and the structural quality of the CdS layer needs to be identified in detail so that the level of Cu_2S quality required for 10- to 20-year life can be established.

Stability and Ternary Chalcopyrite Photovoltaic Devices, L. L. Kazmerski, Solar Energy Research Institute

Work on the copper ternaries ($CuInS_2$, $CuInSe_2$, and $CuInTe_2$) with CdS for photovoltaic devices is in its infancy. Relatively little is known about the compatibility of these materials in a device context and much materials work needs to be done. More work is also needed to understand how methods of deposition, growth, and treatment of ternary films critically affect the cell's structural and electrical characteristics and their relevancy to cell stability.

Major causes for Cu-ternary/CdS device degradation are various impurity diffusion and interdiffusion reactions, which are aggravated by grain boundaries in the polycrystalline films. The high diffusion coefficients reported for Cd and other elements in Cu-ternary/CdS heterostructures, because of the number of vacancies in the ternary, pose potential reliability problems. Fast diffusion of metals into the ternaries can undermine contact stability. Diffusion of oxygen from the ambient during annealing can cause an unwanted oxide layer to form at the interface between CdS and the Cu-ternary. And, rapid diffusion of electrically active defects can cause a rapid increase in electrical conductivity of the ternary.

Stability of Thin Film Polycrystalline Silicon Solar Cells, T. L. Chu, S. S. Chu, and E. D. Stokes, Southern Methodist University

Preliminary results of the stability of thin film polycrystalline silicon solar cells prepared on metallurgical silicon substrates were described.

The temperature coefficients of the cell parameters are similar to those for single crystal silicon solar cells. Exposure to 115°C for up to 160 h, temperature cycles from -40°C to 100°C, and high humidity resulted in no significant change in cell parameters. Exposure to an irradiance of 1.2 W/cm^2 at 150°C under load for 150 h showed some degradation due presumably to a deterioration of grid contacts.

Reliability Studies on MIS and Transparent Oxide-Si Solar Cells, W. A. Anderson and J. K. Kim, Rutgers University

The results of preliminary studies of the stability and degradation of MIS (silicon) and metal-oxide-on-silicon heterojunction[2] solar cells was described. The few previously reported results of degradation studies of MIS cells using silicon were reviewed, recent environmental stress and Auger analysis data on Cr/oxide/Si systems were reported, and some degradation results obtained by R. L. Anderson of the conducting metal oxide materials SnO_2, In_2O_3, and In_2O_3:SnO_2 (indium-tin oxide) on silicon cells were mentioned.

The degradation of tin-oxide-on-silicon heterojunction solar cells is attributed to field assisted transport of O_2^- from the metal oxide to the silicon to form a SiO_2 layer at the interface and adversely affect the series resistance, fill factor, and V_{oc} of these cells. Aluminum contact degradation has also been observed.

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[2]The metal oxide forms a junction with the semiconductor and also acts as a low resistance, transparent contact.

The major degradation problem in MIS cells is the alteration of the oxide interfacial layer due to exposure to air and moisture. Examples of the growth of layer thickness beyond optimum thickness were shown for Au on n-type Si and for Al on p-type Si where moisture trapped in the oxide during formation led to the growth of an aluminum oxide.

Some general observations were made: Hermetic sealing of MIS cells is needed to prevent air and moisture from degrading the oxide interfacial layer and also from degrading the conductance of thin metal films and contacts to these films. Encapsulants are needed which do not discolor or soil during extensive outdoor use. Also, encapsulants need to be studied for their long term performance.

Stability of Conducting Oxide/Si Heterostructure Solar Cells, S. L. Franz, M. L. Andren, and R. L. Anderson, Syracuse University

Extensive results of the degradation of conducting oxides on silicon cells were described. Both heterojunction and heteroface (oxide serves as window only) cells were considered.

The prominant degradation mechanism for SnO_2 on Si heterojunction cells is the formation of a high resistance SiO_2 layer at the SnO_2-Si interface at room temperature. In_2O_3-Si interfaces also degrade in this way but only at elevated temperatures. For both conducting metal oxides, the degradation proceeds more rapidly for polycrystalline silicon than for single crystal cells. Degradation of the In_2O_3:SnO_2-Si interface for both heterojunction and heteroface cells does not occur at temperatures below 470°C. This high threshold temperature allows the annealing of process-induced defects in the silicon and makes promising the use of this conducting oxide for both n- and p-type Si heteroface cells.

Degradation of aluminum electrical contacts to the conducting metal oxides can be prevented by using a chromium barrier.

Unique Problem Areas in M-I-S Solar Cell Structures, S. J. Fonash, G. Fishkorn, and T. E. Sullivan, Pennsylvania State University

While the MIS solar cell design holds promise for use with polycrystalline and amorphous semiconductors, there are a number of problems whose importance is affected by the material system selected and fabrication process used. These problems are related to chemical and electronic effects at the insulator-semiconductor interface and film structure effects.

The electronic nature of the semiconductor surface can undergo considerable changes as an oxide is grown or an insulator is deposited. These changes can be desirable or undesirable depending on the material system used. The problems encountered with a Pd-oxide-n-type Si system were described.

The performance of an MIS cell can be strongly affected by the rate, method, and material of the metal film deposition as well as the surface condition of the semiconductor. A case in point is that while Ag films of good quality can be deposited on Si, Ag deposited on Si having 20 to 30 nm of oxide can lead to a porous film. Such a film leads to high sheet resistance and provides openings for covering materials and the ambient to reach and degrade the junction.

The selection of the semiconductor can also be important: while considerable slow trapping of charge induced by current and causing hysteresis effects has been observed in GaAs, it has not for Si-based systems.

A polycrystalline GaAs/Ge/steel AMOS solar cell system now under development at JPL was described. Two areas under exploration are the passivation of the Ge/steel interface and various combinations of barrier metals and interfacial oxides. Life testing with several metal-oxide combinations has only recently been initiated using 100°C laboratory air environments. Examples were given of cases where the choice of barrier metals such as Ag, Ni, and Cu can be important not only for cell reliability but for efficiency as well. The choice of oxides such as native oxide, MoO_3, and Sb_2O_3 can have marked effects on the cell V_{oc}, fill factor, and stability. Additional experiments are needed (1) to study other deposited oxides with Ga-saturated metals, particularly with reproducible stoichiometric oxides, and (2) to identify metal-oxide-GaAs systems with potential high reliability.

Reliability Testing of GaAs AMOS Solar Cells, R. J. Stirn, Jet Propulsion Laboratory

Preliminary measurement results of the temperature dependence and stability of polycrystalline GaAs solar cells were reported. The change with temperature of V_{oc} and conversion efficiency of gold barrier MIS polycrystalline GaAs cells were found to be similar to those of single crystal GaAs p-n junction cells, while silver barrier cells were found to have higher temperature coefficients. Storage at 60°C for 24 h left the I-V characteristics of gold-barrier cells essentially unchanged but left those of the silver-barrier cells with evidence of increased series resistance. Gold barrier cells were operated under an irradiance stress of $\sim$325 mW/cm^2 at a temperature between 50 and 55°C for more than 48 h. While some degradation of room temperature cell performance was noted immediately after stress, complete recovery was noted after a few hours.

Stability of Thin-Film Gallium Arsenide Solar Cells, S. S. Chu, T. L. Chu, H. T. Yang, and E. D. Stokes, Southern Methodist University

Hydrogenated amorphous silicon solar cells should be stable under normal operating conditions. The results of a number of experiments to explore the stability of amorphous silicon were described. The evolution of hydrogen (applicable at temperatures above about 350°C) will not be a problem at 100°C. The diffusion of dopants such as P and B will not be a problem even at deposition temperatures as high as 300 to 350°C. Electrode materials such as Cr, Mo, Nb, and Ta exhibit little evidence of diffusion, even at temperatures of 400°C. The use of Al and Fe, however, will require care. Iron silicides may form at a fabrication temperature of 400°C to create a large series resistance, while at 300°C the diffusion coefficient is low enough to prevent this formation. Aluminum interdiffuses at 300°C and has been reported to induce crystallization of amorphous silicon at 335°C. The presence of an oxide layer on Al inhibits this interdiffusion, but it also creates a large series resistance.

Stability Studies of Amorphous Silicon Solar Cells, D. E. Carlson, RCA Laboratories

Good stability of devices made with Schottky barriers and of p-i-n cells using other than native oxides was reported. MIS devices utilizing the native oxide as a thin insulating layer exhibit degradation when exposed to air, but this can be reversed by heat treatment.

Session II: Measurements and Tests Used to Define Stability in Related Technologies

The experience of the silicon cell space program and its implications for thin film cells were presented. Most of the methods used to ensure stable space cells are ruled out for terrestrial application because of the costs involved. On the other hand, efforts made in the space cell program to develop a spirit of cooperation between cell makers and users and to select realis-

Silicon Cell Space Program Experience, P. A. Iles, Optical Coating Laboratory, Inc.

tic tests will be even more important in the thin film cell program.

The wide range of possible materials and processes for thin film cells will make difficult the early utilization of automated production (which will probably be needed to achieve low-cost goals). It will also make complex the task of developing tests to measure the stability of these many cell types.

The use of thin film materials can present major problems in attempting to achieve long cell life. For all thin film cells, the contacts will pose a major problem due to initial requirements (low cost and good conductivity) and stability needs (freedom from corrosion and failure under temperature cycling). Also, problems should be expected from interlayer movements of material during cell life, with their adverse effects on cell properties.

Effective methods of encapsulation will need to be developed to reduce the degradation effects of the atmosphere on cells. Also, the search for metallurgically stable systems must be continued.

Reliability Concerns and Life Test Procedures for Concentrator Solar Cells, W. V. McLevige, Sandia Laboratories

Reliability concerns and life test approaches for concentrator solar cells were described. Reviewed were the many stressful operating and environmental conditions that concentrator cells must sustain which hold the possibility of many causes for degradation. Just how serious these stressful conditions may be remains to be seen because only limited life test data are presently available.

The three most basic accelerated tests used and ones that were recommended for consideration are those involving constant temperatures, temperature-humidity cycling, and temperature-illumination stresses. Some preliminary results were described of recent accelerated tests on Si and AlGaAs/GaAs concentrator solar cells. These examples were provided for their tutorial value in demonstrating the kind of information that can be obtained from such tests.

Some Reliability Problems in Integrated Circuits - Their Detection, Definition, and Remedy, J. W. Adolphson, NASA/Goddard Space Flight Center

Some of the reliability problems encountered in integrated circuits were reviewed to alert the photovoltaic community of potential pitfalls and to advise it of ways to view the reliability problems to help achieve solar cell stability.

Proper device design and fabrication are not only necessary to achieve the desired functional performance but also the desired reliability. The need to assure that reliability is built in the device has led to, for example, the use of the scanning electron microscope to check the quality of metallization interconnections. The introduction of such a sophisticated instrument on a manufacturing processing line was revolutionary at the time, but its use is now an accepted fact. The ability to detect problems with this instrument early in the manufacturing process led to production cost savings and to process changes that have resulted in inherently more reliable devices.

In summary, the importance of user involvement was emphasized. Involvement means a heightened awareness of device design, processing, manufacturing, testing, and device specification. Additionally, it means the development of capabilities to perform product evaluations and failure analyses. And, it implies coordination and cooperation not only with other users but with manufac-

turers themselves to promote product reliability and standardization.

Tests for Instabilities in Silicon Integrated Circuits, C. W. Green, Bell Telephone Laboratories

The major degradation and drift phenomena of integrated circuits and the tests which can be used to uncover them were reviewed. While these tests can reveal problems, sophisticated analytical techniques are necessary to thoroughly understand and to control the processing and material parameters which lead to instabilities and degradation.

Most of the instabilities encountered in integrated circuits are functions of electrical bias, humidity, or temperature and can be accelerated by subjecting the devices to the application of extraordinary levels of these stresses. Tables were reviewed which summarize the types of tests expected to be useful in identifying devices afflicted by the various drift and degradation mechanisms.

Because of the complexity of integrated circuits, it is impractical to subject all sensitive components to stressful conditions of accelerated life tests to predict long field service. Insight into device quality and reliability is acquired from a combination of using selected stress tests, thorough analysis of the component materials and processes, and assurances that the quality of materials and the processes and devices remain controlled.

Real-Time Controls for Reliability Assurance, S. Kukunaris, RCA

An approach to device stability analysis which can be accomplished quickly and with few samples was described; this approach has been used with transistors and CMOS devices. It is called real-time control testing, and its basis is the use of accelerated testing where the level of stress is selected to maximize the acceleration of degradation mechanisms active during device life. The stress level is selected to be as high as possible without activating failure mechanisms not active during the operational life of the devices tested. This stress level can be selected with assurance only when an information bank is available which consists of the results of extensive traditional efforts in life testing, stress testing, failure analysis, and field use.

Interdiffusion and Interface Problems Relating to Thin Film Photovoltaic Devices, L. L. Kazmerski, Solar Energy Research Institute

Interdiffusion and interface problems were reviewed which are related to thin film polycrystalline photovoltaic device performance and stability. These problems are aggravated by enhanced interactions at grain boundaries. It was cautioned that while the diffusion processes have been much studied by a variety of techniques, these studies have sometimes been conducted with mixed success and skill. The relatively recent development of surface analysis techniques and the use of two in particular, Auger electron spectroscopy and secondary ion mass spectroscopy, have highlighted interdiffusion investigations, however.

The three major interface problem areas were considered: the grid contact to the semiconductor, the semiconductor to semiconductor junction, and the semiconductor to back contact region. Representative problems were cited for a number of material systems: InP/CdS, GaAs, amorphous Si, Cu_2O, Cu_2S/CdS, Cu-ternaries, and SnO_x/Si. With these examples it was concluded that much work needs to be done in controlling interdiffusion mechanisms in thin film polycrystalline solar cells so that these degradation processes can be minimized.

Corrosion and Its Control, R. P. Frankenthal, Bell Laboratories

The conditions for which electrolytic, galvanic, and stress corrosion can develop were reviewed. Many corrosion problems can be avoided by the proper choice of materials and device design, and by rigorous efforts to avoid moisture and ionic contamination. Moisture can reach the device surfaces either as a result of exposure of parts to moisture prior to or during device processing, by diffusion through encapsulants (most encapsulants used are permeable to water), or by ingress through faulty seals. Only minute amounts of ionic contaminant residues on surfaces, due to inadequate cleaning procedures, can greatly increase the rate of corrosion where moisture exists.

Corrosion failure modes mentioned are increased resistance of conductor stripes, short circuits due to dendritic formations, and increased leakage currents due to the spreading of corrosion products between conductors.

Two other noteworthy observations were made. No metal is immune from corrosion, given the right conditions; and many instances of corrosion can be attributed to dust particles from the atmosphere.

Terrestrial Silicon Array Field and Test Experience, R. G. Ross, Jr., Jet Propulsion Laboratory

Experiences in the Low-Cost Solar Array Project with silicon flat-plate solar cell modules were described. Six key failure modes have been identified from field experience. They are: electrical interconnect breakage, metallization deterioration, electrical insulation breakdown, solar cell cracking, encapsulation cracking and delamination, and optical surface soiling. It is probable that they will be important in thin film arrays also. Problems with the first three have been substantially solved, while considerable progress has been made with the others.

Qualification tests have been used to evaluate design solutions to address various failure modes. Some of the problems in the selection of meaningful environmental test stresses were discussed, and the relative value of the environmental tests used were reviewed. Thermal cycle, humidity, and structural tests have proved to be of great value, while ultraviolet stress tests have been difficult to interpret. Research on ultraviolet-humidity, bias-humidity, and module soiling tests is under way.

Methodology for Designing Accelerated Aging Tests for Predicting Life of Photovoltaic Arrays, R. E. Thomas and G. B. Gaines, Battelle-Columbus Laboratories

Recently proposed concepts and methodology for designing accelerated tests for silicon solar cells were highlighted. The basic approach is equally valid for the accelerated testing of thin film cells, although accelerated tests for thin film cells will likely have to be designed to be specific to each of the different cell types. Among the aspects of this design approach is the requirement of using only "mature" devices made by well-controlled fabrication processes, the availability of a broad range of data on device experience, engineering judgments based on these data to assess the relative severity of various combinations of stresses that need to be considered, an approach for uncoupling different failure mechanisms, a suggested time-acceleration factor of ten, and the use of at least five stress levels for each type of stress.

Session III: Discussion Group Sessions to Identify Tests and Measurement Procedures That Can be Used to Enhance the Prediction of Material and Device Stability

Discussion Group I on Cu_2S/[CdZn]S and Amorphous Si, L. L. Kazmerski, Solar Energy Research Institute, and J. D. Meakin, Univ. of Delaware

Several general aspects of measuring and reporting cell and material characteristics and stability were discussed. As a guide to what to expect of the types of cells under discussion, the following five classes of degradation mechanisms were developed and discussed: interdiffusion (implies mass transfer), chemical (oxidation, corrosion, or other chemical state change), electrolytic (decomposition due to field-induced ion motion), mechanical (such as grid lift-off, delamination, etc.), and photochemical (which encompasses any cell change which is directly induced by photons).

To allow for the development of a meaningful data base on which to assess test results of others and to evaluate cell stability, substantial agreement was reached in defining what conditions should be reported and the circumstances under which it is necessary to specify the test method details. Some of the general test conditions identified are insolation, temperature, stress, electrical loading, and ambient. Also cited was the importance of providing complete information about the experimental design and the characteristics of the cells before the initiation of the tests. The group also felt that to intercompare the performance of cells from different organizations and production periods, it would be better to establish a set of test procedures to which all would adhere than to establish a central test facility, as has been suggested by some.

A number of aspects and considerations regarding accelerated tests were discussed. To be able to project long term performance of cells, it will be necessary to establish functional relationships between test stresses and the degradation mechanisms to be accentuated. Also, the synergistic effects of different stresses to a given degradation mechanism cannot be ignored. Furthermore, the need to extrapolate long term cell stability from small changes in characteristics resulting from stress tests over a relatively short testing time places considerable importance on the precision of the test methods used to measure these changes. The paper presented in Session II on the methodology for designing accelerated aging tests for degradation mechanisms stimulated considerable discussion about its application to thin film cells. While the potential value of this approach was appreciated, some members of the group felt that the use of five stress levels, which was recommended, would require an excessive amount of testing.

Discussion Group II on Polycrystalline Si, MIS, and Conducting Oxide/Si, J. Schewchum, McMaster University, and R. L. Anderson, Syracuse University

An extensive and far-reaching set of research needs was developed which reflects both the breadth of cell designs and the immaturity of the material, cell, and measurement technologies involved. What is needed, basically, is a better understanding of and an improved measurement capability for virtually every aspect of these cells.

The material parameters of the various classes of polycrystalline silicon pertinent to solar cell performance need to be identified. Measurement standards of polycrystalline silicon are needed to allow for more meaningful assessment of data being reported. In particular, methods to measure the following were cited: resistivity, mobility, lifetime, diffusion length, grain

size and orientation, void space between grains, and impurity content within grains and at grain boundaries.

Guidelines are needed to measure the various aspects of interfacial layers such as interfacial resistance, variation of thickness with time, pinholes, impurity composition, and density and energy of charge states.

A better understanding is needed of the various reactions at interfaces; of the influence of grain boundaries on the mechanical and electrical properties of materials and cells; of the effects of built-in and applied electric fields; of the compatibility of the various material combinations; of interdiffusion phenomena at interfacial layers, window interfaces, and grain boundaries; of conducting window materials; and of the encapsulants used.

Indicative of the relative immaturity of the technology for these cells, the need to understand better the operation of these cells and to understand their degradation mechanisms was emphasized. As a consequence, there is a need to identify which parameters affect most the energy conversion efficiency of these cells. Also, ways are needed to predict the potential conversion efficiency of various material systems to determine which are worth developing.

Regarding the matter of long term stability, it was felt that all mechanisms encountered in single crystal homojunction solar cells must be considered. To these must be added degradation mechanisms related to any possible incompatibilities of the various materials used, including encapsulant materials. The classes of degradation mechanisms identified by the group are essentially identical to those identified by Discussion Group I. Because of the great differences in the material systems, it will not be possible to have accelerated test standards applicable to all cell types. Initial approaches in developing these standards should, however, be based on those for single crystal silicon cells. To accelerate the development of a data base, laboratory and use tests should be conducted concurrently. Tests on unprotected cells, insofar as that is possible, should be made to assist in discovering intrinsic degradation mechanisms.

Discussion Group III on Thin Film GaAs, R. J. Stirn, Jet Propulsion Laboratory

Thin film GaAs solar cell technology was considered to be sufficiently immature to require the discussions to be oriented more to understanding the various mechanisms at play in these cells than to address the question of predicting cell lifetime. Three broad topic areas were examined: classes of degradation, test strategies to uncover degradation problems, and areas where more research is recommended.

Regarding degradation, three major classes of phenomena were identified and discussed: interdiffusion, chemical, and mechanical.

Under interdiffusion phenomena are a plethora of effects, for example: degradation of the contacts between the GaAs and the substrate and the front metallization; reactions involving the barrier metal, interfacial oxide, and bulk GaAs; degradation of conducting oxide layers; and reactions at grain boundaries. Under the category of chemical effects were mentioned front contact corrosion and interfacial oxide modification problems. Under mechanical effects were potential problems with the strength and integrity of the front contacts and interconnects, especially in

Schottky barrier-type cells where bonds to a thin metal film are required.

A number of screen, operating, and accelerated tests were suggested to reveal some of the above degradation modes. They involved the use of I-V characteristics, as a function of temperature, and the use of changes in spectral response to reveal cell degradation, in the process of subjecting cells to temperature cycling and high temperature storage stresses. High humidity is added to accentuate those stresses.

Four general areas of research were called out as requiring extra attention to promote the development of viable cells. The most crucial area is in the selection of the low cost substrate and its treatment. Research is also needed to better understand the interfacial oxide layer and barrier metal alloys of these cells, to investigate more cost-effective means of manufacturing GaAs, and to study the making of electrical contacts to thin films with adequate bond strength and low contact resistance that do not lead to shorted junctions or degraded Schottky barriers.

THE IMPORTANCE OF THIN FILM SOLAR CELL STABILITY

D.L.Feucht, Chief
Advanced Material R&D Branch
Division of Solar Technology
U.S.Department of Energy

The overall objective of the National Photovoltaic Program is to ensure that photovoltaic conversion systems play a significant role in the Nations energy supply by the year 2000. In order to achieve this overall objective, photovoltaic flat-plate modules or concentrating arrays must be produced for a price of $0.10 to $0.30 per peak watt by 1990, (in 1975 dollars). The development of thin-film solar cells and materials is vital to the achievement of this goal. These cells must not only have a reasonable efficiency, (approximately 10%) but must provide reliable operation for a life of at least 20 years. In order to achieve this long life it is necessary that the stability and reliability of thin-film cells be addressed early in the research and development cycle.

The Advanced Materials R&D Branch is investigating a variety of materials which have the potential for achieving the desired conversion efficiency, low cost and lifetime. The particular phenomena which limits the life of any given cell may well be a function of the particular material syste Thus, while general tests may be developed to determine the reliability of a cell or an array,diagnostic tests specific to an individual material system will be required in order to determine the phenomena limiting the cell life. The purpose of this Workshop is to identify and discuss the problems and obstacles to achieving 20 year reliability for thin-film solar cells, to consider how these may be overcome, and to discuss test an measurement procedures which can be designed to enhance the prediction of material and device stability. The results of this workshop will play an important role in determining the directions of the future reliability and stability activities of the Branch.

Status of the DOE Photovoltaic Performance Criteria and Standards Project

Dr. Leonard M. Magid
Division of Solar Technology
U.S. Department of Energy

The first figure lists the overall objective and the latest array-price and electric system energy cost goals of the U.S. Department of Energy's (DOE's) Photovoltaic Program, as given in the recently released National Photovoltaic Program Plan, dated March, 1978.

A key element of this plan as far as this workshop is concerned is the newly created Performance Criteria and Standards Project. The Solar Energy Research Institute (SERI), of Golden, Colorado, has been assigned the lead management role for this project, with Gary Nuss, Chief of the SERI Technology Evaluation Branch, as its manager. The second and third figures give some early planning objectives and milestones for this effort.

SERI will be working with the Photovoltaic community, NBS and appropriate standards groups to develop this program element.

PHOTOVOLTAICS

OVERALL OBJECTIVE:

To ensure that photovoltaic conversion systems play a significant role in the Nation's energy supply by stimulating an industry capable of providing approximately 50 GWe of installed electric generating capacity by the year 2000.

BASIC GOALS:

- o NEAR TERM (1982): $2/peak watt array price @ 20 $\frac{MWP}{YR}$ for 100-200 mils/kWh
- o MID TERM (1986): 50¢/peak watt array price @ 500 $\frac{MWP}{YR}$ for 50-80 mils/kWh
- o FAR TERM (1990-2000): 10-30¢/peak watt array price (1990) 10-20 $\frac{GWP}{YR}$ (2000) for 40-60 mils/kWh

PROPOSED PLAN

PHOTOVOLTAIC PERFORMANCE CRITERIA AND STANDARDS PROJECT

OVERALL OBJECTIVE:

To stimulate the development and adoption of industry established photovoltaic material, component, subsystem and system performance criteria and standards for the design, production, sales and operation of reliable, safe and high quality power systems.

SPECIFIC OBJECTIVES:

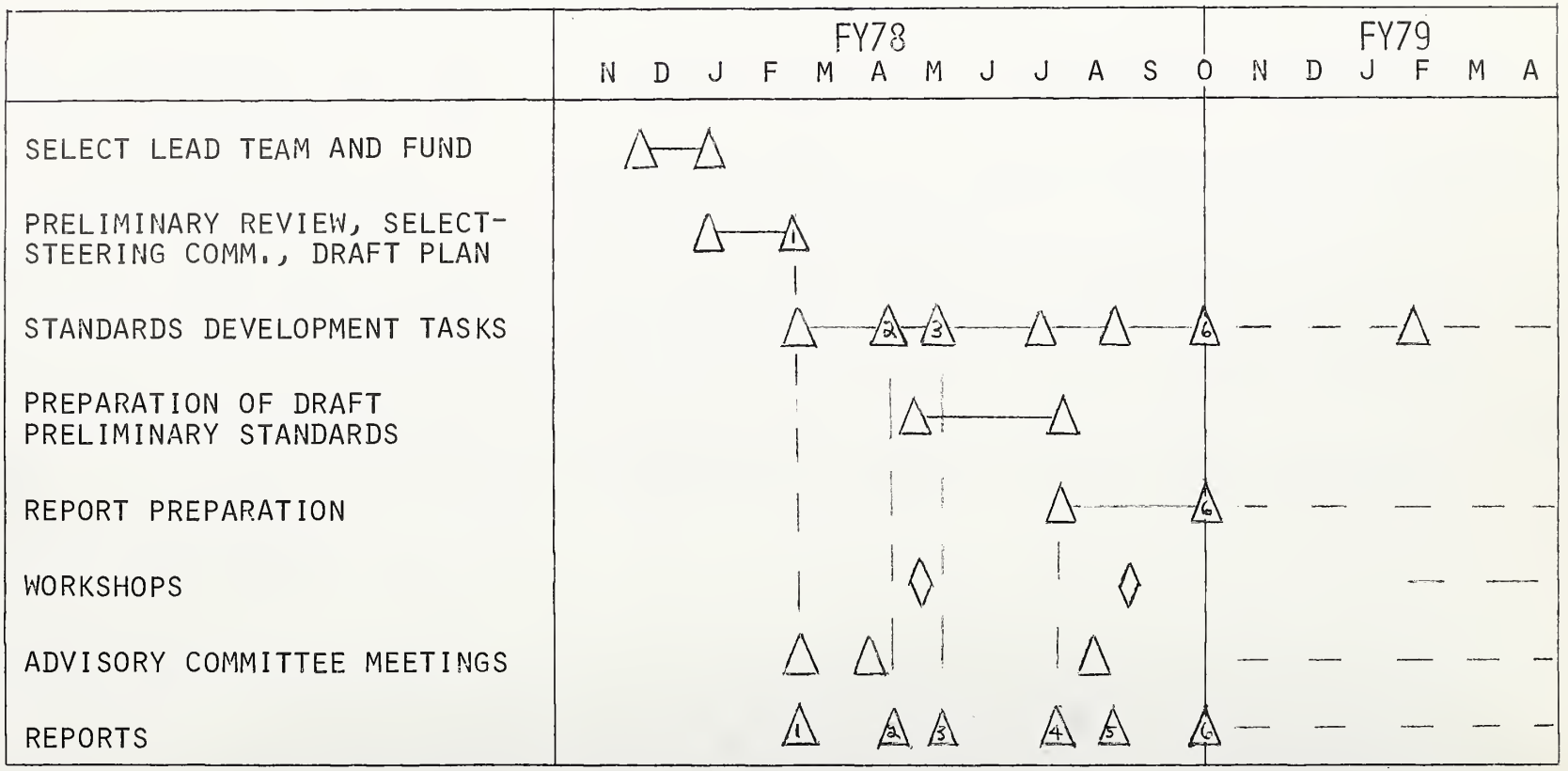
FY78:
- o To identify, prioritize, develop and publish the preliminary performance criteria and standards needed for the continued growth of photovoltaic applications within the private sector.
- o To encourage the early involvement of industry and professional societies in the photovoltaic standards development and adoption process.

FY79:
- o To establish procedures for the identification and accreditation of qualified photovoltaic testing laboratories.
- o To assist in the development and adoption of interim photovoltaic performance criteria and standards.

FY80:
- o Industry adoption of photovoltaic performance criteria and standards.
- o To assist the state and local regulatory community in the review and approval of photovoltaic health, safety and performance codes.

PROPOSED SCHEDULE

PHOTOVOLTAIC PERFORMANCE CRITERIA AND STANDARDS PROJECT



1 - INITIAL STANDARDS DEVELOPMENT PLAN (SDP)

2 - DRAFT STANDARDS DEVELOPMENT PLAN

3 - STANDARDS DEVELOPMENT PLAN

4 - COMPILATION OF INITIAL PC&S DRAFT

5 - REVISED PC&S DRAFT

6 - ISSUE PRELIMINARY PC&S PROCEDURES

4. Presentations in Session I: Status of Present Reliability Testing, Failure Modes, Failure Mechanisms, and Data for Advanced-Cell Materials

THE STABILITY AND RELIABILITY OF CdS/Cu_2S SOLAR CELLS

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I. Introduction

A photovoltaic effect in CdS was first reported in 1954 by Reynolds[1] for a junction made by electroplating a film of copper onto an indium doped CdS crystal and then heating the crystal to 350°C. Later work established that the junction was between CdS and Cu_2S.[2] A great number of research and development efforts have followed since this initial discovery with the majority focused on thin film polycrystalline cells for either space or terrestrial use. An exhaustive review of the work up to 1973 has been published by Stanley.[3]

Many different cell designs have been developed and a wide variety of techniques used to deposit the constituents and to make electrical contacts. However, since the National Aeronautical and Space Administration sponsored work at the Clevite Corporation,[4] the majority of the effort has been devoted to improving the vapor deposited thin film polycrystalline cell first developed in that program. The cell is constructed by vapor depositing a 20 to 40 μm thick CdS layer on a thin metal substrate or a metallized plastic film. A short etch in hydrochloric acid produces a heavily textured light trapping surface which is then reacted in a CuCl solution to produce a layer of Cu_2S 0.1 to 1.0 μm thick. The top electrical contact is then generally made with a metal grid using a variety of techniques such as vapor deposition, electroplating or pressure contacting.

Many features of the structure and operation of the cell were unknown or poorly understood during the first twenty years or so of development. Major difficulties were encountered in the reliable production of high efficiency cells and many cells were found to be unstable and rapidly decayed below their initial efficiency. Lack of knowledge on the structure and operation of the cell, as first produced, resulted inevitably in an almost bewildering range of mechanisms being proposed to explain the observed decay in performance with time.

Figure 1 shows a schematic cross section of a typical vapor deposited thin film CdS/Cu_2S cell. This figure shows a front wall cell (light incident through the Cu_2S); backwall cells utilize a transparent conducting layer for the substrate e.g. SnO[5] or $CdSn_2O_4$[6] on glass and the top contact can then be replaced by an opaque conductor. The basic operation of the CdS/Cu_2S heterojunction has now been well established and is reviewed in detail by Rothwarf and Barnett.[7] The ideal efficiency for the CdS/Cu_2S junction without any losses is ∿ 16% and the practical achievable efficiency is estimated to be 11%. Cells of a conversion efficiency above 9.0% have been reported by the Institute of Energy Conversion of the University of Delaware.[8] Figure 2 shows the band diagram that is believed to apply to

high efficiency CdS/Cu_2S cells.

Almost all the photon absorption and minority carrier generation takes place in the Cu_2S layer. The generation efficiency is determined by photon losses and the minority carrier loss mechanisms such as surface and bulk recombination in the Cu_2S and interface recombination at the CdS/Cu_2S junction. Measured short circuit currents have shown that the Cu_2S surface is generally well passivated and that bulk recombination rates are strongly dependent on the Cu_2S stoichiometry. The effectiveness of interface recombination depends on the balance between the drift field in the CdS, F_2 and the interface recombination rate S_I. Rothwarf [9] has shown that the fraction of electrons successfully crossing the interface is given by

$$\mu F_2/(S_I + \mu F_2)$$

where μ is the electron mobility in the CdS. Measurement of dark and light capacitance has shown that the collection field is much enhanced in the light as a consequence of hole trapping in the junction region (Fig. 2).

The open circuit voltage achievable is limited to about 0.57 V by the electron affinity mismatch between Cu_2S and CdS indicated in Figure 2. In addition, V_{OC} can be further reduced by junction area effects and high field regions.[7] Good cells show diode factors of 1 and hence the fill factor can in principal be as high as 80%; inhomogeneous fields and series and shunt resistances reduce the achievable fill factors to the 70-75% range.

2. CdS/Cu_2S Life Testing

The early life testing of thin film CdS/Cu_2S cells was aimed at establishing performance data relevant to space missions. Measurements of electrical performance were made at various temperatures under a range of illuminations. In addition, severe thermal cycling tests were conducted to simulate space mission conditions. Definitive analysis of the life performance data was hampered in many cases by the poor reproducibility of cell production and by the still developing understanding of the cell structure and operation. The large spread in initial cell properties was reflected in a wide variation of apparent cell stability.

Work under National Aeronautical and Space Administration sponsorship at the Clevite Corporation has been summarized in a number of publications.[4,10,11] A major result of the NASA studies was the identification of copper nodule growth as a primary degradation mechanism. Cells exposed to light under open circuit conditions were found to degrade rapidly and microscopic examination of cell cross-sections identified copper filament and nodule growth as the cause of the decay. Tests on cells loaded to various voltages indicated that a threshold voltage between 0.35 and 0.4 V[9] was necessary to cause copper nodule growth for the type of cell under test.

The Boeing Aerospace Corporation conducted a number of stability studies of Clevite cells for NASA[12] The cells were either maintained at 55°C under constant illumination or were cycled for 60 minutes illumination, 30 minutes darkness resulting in a temperature cycle from -100°C to 60°C. Cells were

illuminated by a Xenon simulator while maintained in a dynamic vacuum of $\sim 10^{-6}$ torr; the cells were loaded to close to the maximum power point. No attempt was made to analyze the cause of failure or degradation. It was concluded that the most significant parameter controlling the rate of degradation was the date of manufacture of the cell suggesting that structural and compositional factors were dominant. No significant differences were detected between continuous and intermittent illumination. Testing covered the range from 2,500 to 15,000 hours and resulted in efficiency losses from as little as 3% to as much as 29%. One or two cells even showed a 1 or 2% increase in efficiency. It should be noted that the initial power conversion efficiencies were generally in the range of 2 to 3%.

Researchers at a number of laboratories in France have made major contributions to the understanding and control of cell degradation. In 1973[13] the full importance of the stoichiometry of the Cu_2S layer was recognized and the loss of stoichiometry by oxidation was established. Life testing showed that the degradation rate was slower at better vacuums. Doping of the CdS with an unspecified dopant was also reported to result in improved stability even under open circuit conditions. Extended test results on the 1973 cells were recently reported.[14] Table 1 shows the results of exposing

Table 1

Life Testing of CdS/Cu_2S Cells[14]

Exposure to AMO at 60°C under Vacuum for 7000 Hours
Initial CdS/Cu_2S Efficiency $\sim$ 6.7%

Cell	$\Delta J_{sc}/J_{sc}$	$\Delta FF/FF$	$\Delta\eta/\eta$
CdS/Cu_2S - Kapton	-8.3%	+2.0%	-7.5%
CdS/Cu_2S - Aclar	-37.3%	+0.3%	-39.3%
Silicon - Aclar	-34.0%	-1.5%	-37.2%

Exposure to 95% Relative Humidity at 40°C for 5000 Hours†

Cell	$\Delta J_{sc}/J_{sc}$
CdS/Cu_2S - Aclar	90%
CdS/Cu_2S - Glass	1%

cells to AMO at 60°C under a dynamic vacuum. Much of the efficiency degradation noted for the Aclar covered cells can be attributed to loss of transparency of the Aclar. Kapton is a more satisfactory cover but is not sufficiently impervious to prevent loss in performance. Cells hermetically sealed behind glass do however seem to be essentially stable under the conditions tested. After 5000 hours at 40°C and 95% relative humidity, the short circuit current has declined by only 1%, a change that is probably

† Illumination not specified.

within the experimental error. The 7000 hour test was stated to be equivalent to six years terrestrial deployment.

Corroboration of the French results is provided by the tests of Clevite cells performed by Westinghouse.[15] Groups of cells were sealed behind glass and maintained at 40, 60, 80 and 100°C. The cells were loaded to the maximum power point and illuminated at AM1 for a 12 hours on 12 hours off cycle. The decline in the average efficiency of groups of four cells after 18 months exposure was 3.4, 0, 3.1 and 32% at 40, 60, 80 and 100°C, respectively. In all cases, the fill factors declined (3.6, 4.3, 12.1, 29%) but at 60 and 80°C this was offset by substantial improvements in short circuit current.

Various accelerated and roof top tests have also been conducted at I.E.C.[16] on Clevite cells and also on cells produced at I.E.C. under NSF/RANN sponsorship. Cells were maintained in a variety of flowing gasses at various temperatures and exposed to simulated AM1 illumination either continually or for one hour on one hour off cycles. All cells maintained in dry air degraded more than 20% in seven months. Considerable variability was observed in the cells maintained under Argon or Nitrogen with a few cells showing negligible degradation after seven months.

The life testing briefly reviewed above has shown conclusively that cells will generally degrade rapidly if exposed to air. In the following section, evidence will be reviewed which shows that such degradation is at least in large part due to oxidation of the Cu_2S layer which lowers the stoichiometry of the Cu_2S layer. Cells well protected from oxidation by either dynamic vacuums or by encapsulation behind glass have shown minimal degradation rates implying that the basic heterojunction structure is capable of long term stability. Probably the longest "test" on record was reported by D. C. Reynolds[17] for an epoxy encapsulated array of 18 back wall single crystal cells made by the Harshaw Company in 1957. No special precautions were taken to store the array and testing 17 years later showed no detectable degradation from the original performance of 8.2 V open circuit voltage and 9.5 mA short circuit current.

Until stability measurements under deployment conditions can be interpreted in terms of specific degradation mechanisms, projections of usable lifetimes are at best subject to considerable uncertainty. This is even more true of efforts to use accelerated life testing to forecast deployment lifetimes. Such testing will be discussed further in Section 4.

3. Analysis of Degradation Mechanisms

Oxidation of Cu_2S

The loss of cell performance caused by oxidation of the Cu_2S is probably the most definitively established degradation mechanism and is responsible for many of the early reports of cell instability. The reaction is, however, reversible and can be expressed as follows,

$$Cu_2S + \frac{\delta}{4} O_2 \rightleftharpoons \frac{\delta}{2} Cu_2O + Cu_{2-\delta}S.$$

Under oxidizing conditions, the heat of formation of the Cu_2O will drive the reaction to the right but under strongly reducing conditions, the reaction is reversed and the initial stoichiometry can be restored. Figure 3 shows that little oxidation is needed to substantially change the stoichiometry of the Cu_2S layers typical of the high efficiency cells now being made at I.E.C. A discussion of the influence of Cu_2S stoichiometry on short circuit current and Cu_2S sheet resistivity is presented elsewhere.[9] It is sufficient for present purposes to point out that virtually the highest achievable stoichiometry and the concomitant highest sheet resistivity is necessary to achieve the maximum short circuit current. Figure 4 reveals how rapidly the sheet resistance of unprotected Cu_2S decays in air. The figure also shows partial recovery of the resistivity with a brief reducing heat treatment. A more extensive treatment will fully restore the resistivity to the initial value. Figure 5 shows how the actual I-V behavior of a cell is degraded by oxidation and can be restored by a reducing treatment.

Diffusion of Cu into CdS

It is well established that copper diffuses from the Cu_2S into the CdS and results in a compensated region. Measurement of the dark capacitance as a function of time and temperature have been used to estimate the width of the compensated region[18] and to determine the diffusion coefficient of Cu in CdS. Excessive copper diffusion has been suggested as a cause of degradation and estimates of usable deployment life have been made assuming standard thermal activation relationships.

A number of mechanisms have been proposed to explain loss of performance because of copper diffusion. It has been suggested that the series resistance contribution of the compensated region will become sufficient to lower the fill factor.[4] Other suggestions are that the loss of copper from the Cu_2S or the reduced field in the junction region will give lowered short circuit currents.

The gradual widening of the compensated layer is well documented but recent work at I.E.C. has shown that this is not associated with a loss in short circuit current. Table 2 shows that while the dark capacitance declines rapidly with heat treatment, the capacitance under AM1 illumination is changing much more slowly. Trapping of light generated holes near the Cu_2S/CdS junction is believed responsible for the high capacitance in the light (Fig. 2) but the important point to make here is that the field at the junction and hence the current collection efficiency is relatively insensitive to protracted high temperature exposure. Recently made high efficiency cells (> 8.5%) are routinely exposed to 170°C for over 50 hours during manufacture. The contribution of the CdS resistivity to the total cell series resistance has been found to be insignificant even after these protracted heat treatments. Fill factors of over 70% are routinely achieved after heat treatments exceeding 100 hours at 170°C.

Table 2

Influence of Heat Treatment on
Dark and Light Capacitance and Short Circuit Current

Cell #	State	Capacitance nF/cm^2		J_{sc} mA/cm^2
		Dark	Light	
668 A1-1	Initial	12.0	98	15.5
668 B1-1	Initial	18.4	99	16.4
673 A1-1	Initial	11.1	66	16.0
673 B1-1	Initial	12.4	73	18.0
668 A1-1	12 hours, 170°C	8.16	98	15.8
668 B1-1	12 hours, 170°C	9.93	96	17.1
673 A1-1	12 hours, 170°C	5.82	66	16.9
673 B1-1	12 hours, 170°C	6.53	73	17.8
668 A1-1	20 hours, 190°C	2.10	89.1	16.4
668 B1-1	20 hours, 190°C	2.94	88.0	18.0
673 A1-1	20 hours, 190°C	1.35	60.2	18.1
673 B1-1	20 hours, 190°C	1.43	69.5	18.4

Electrolytic Decomposition of Cu_2S

Electrolytic decomposition of Cu_2S is a well documented fact.[19] If a sufficient potential difference is maintained across a chalcocite sample, copper will plate out at the cathode and reduced stoichiometry sulfide will form at the anode. The necessary threshold voltage at the copper deficient boundary of chalcocite, $Cu_{1.995}S$[20] can be computed from thermodynamic data to be 0.265 V. Assuming that the activity of copper varies linearly with composition over the chalcocite phase, the threshold voltage will fall in a linear manner to zero at the Cu_2S boundary where chalcocite is in equilibrium with copper. Actual measurements show a slight overvoltage above the thermodynamic values[19] possibly due to the kinetics of copper nucleation. In an actual cell the major potential drop is across the CdS and only as the Cu_2S approaches ideal stoichiometry can any potential be supported by the Cu_2S. Present knowledge of the relative conductivities of the Cu_2S and CdS layers suggests that the threshold voltage will never be reached. Even if the Cu_2S layer was initially ideally stoichiometric and hence approached an insulator, the increase in threshold voltage as copper plates out at the CdS/Cu_2S junction ensures that the process is self limiting and decomposition would terminate when only a fraction of a monolayer of copper had formed.

The situation is completely different in a structurally imperfect cell where deep cracks or pores in the CdS become coated with Cu_2S. Under these conditions, the Cu_2S layer can be subjected to substantial electric fields resulting in sufficient copper deposition to provide shorting paths to the base electrode. Such copper growths have been directly observed[10] and the existence of deep channels and defects established.[21] In summary, the evidence available suggests that cells constructed on defect free CdS will be immune to electrolytic decomposition of the Cu_2S.

There is an alternative origin of a potential gradient in the Cu_2S which does not seem to have received attention in the literature. With a wide grid spacing, the inhomogeneous current density in the Cu_2S will create a potential gradient from the grid line to the mid-line position. If sufficient potential is developed, this will result in the establishment of a lateral stoichiometry gradient. The impact of this on cell performance and stability remains to be established.

Structural Instabilities

A multi component composite structure such as the CdS/Cu_2S cell can fail or degrade in a variety of structural ways unrelated to the actual heterojunction. The extreme temperature cycling to which cells were subjected during the N.A.S.A. program was shown to cause delamination at the substrate-CdS interface.[10] Many possibly polymeric encapsulants are known to lose transparency and structural integrity when exposed to ultra violet radiation. In retrospect, it is clear that many cell failures were caused by loss of electrical contact between the Cu_2S and pressure bonded gridding systems. Reviewing the current state of knowledge, it is not apparent that there are any structural failure modes which cannot be successfully designed against. There will, however, have to be substantial development efforts to produce both reliable and economically acceptable techniques for cell gridding and encapsulation.

Summary

It is concluded that the research and testing conducted to date has identified the major cell degradation mechanisms none of which preclude the production of cells with usable lifetimes of 10 to 20 years. The quantitative data needed to determine the rate of degradation for terrestrial deployment is generally lacking, due in part to changes in cell design and improvements in initial cell performance. To obtain such data in the short term will require the successful development of accelerated testing procedures which is the subject of the next section.

4. Accelerated Life Testing

In many technologies, it has proved possible to develop highly reliable accelerated testing procedures, e.g. short term creep testing to forecast service life. To do so requires detailed knowledge of the degradation mechanism being accelerated. In the case of thin film solar cells and CdS/Cu_2S specifically, such knowledge is not available. Most of the accelerated life tests to date have utilized elevated temperatures and enhanced illumination (either intensity or duration) to hasten degradation. If indeed there is degradation due to thermally activated processes, then high temperatures will increase its rate. However, before meaningful data interpretation and computation of equivalent lifetimes at deployment temperatures is possible, such activated mechanisms must be identified and thermal coefficients or activation energies determined. Similarly, problems exist in equating five hours of continuous illumination to 24 hours of deployment. Unless it can be shown that degradation occurs solely under illumination or that there are recovery mechanisms active in the dark, such equivalences

are without foundation. The almost universal weakness of all published accelerated life test data is that observed degradation has not been matched to specific changes in the cell. Meaningful accelerated testing will not be possible until specific degradation mechanisms are identified and acceleration procedures matched to the mechanisms.

5. Research Needs

In order to project cell lifetimes under deployment conditions, it is essential to determine the degradation mechanisms taking place and their effect on cell performance. Attention should clearly be focused on those mechanisms which are intrinsic to the junction and which exist in high efficiency cells. There is little merit in laboriously cataloguing the decline of cells which initially had efficiencies below usable levels. If oxidation of the Cu_2S can occur, it is now well documented that this will cause major loss of output. Accordingly, to determine other life limiting effects, the cells tested must be made resistant to this mode of degradation. The following are seen as the major research needs which when satisfied will allow life projections of the CdS/Cu_2S cell to be made with confidence.

1. A quantitative description of the interaction of oxygen with the Cu_2S layer and the associated structural and electronic changes. Associated with this study should be the development of either ideal hermetic sealing or the measurement of diffusion rates through non-ideal encapsulations.

2. The identification of those inter-diffusion mechanisms which reduce cell performance and the measurement of their time-temperature characteristics.

3. The identification of structurally related degradation modes such as delamination and loss of grid contact and their relation to deployment conditions.

4. Identification of the detailed relation between copper nodule formation and CdS structure and properties. Confirmation that nodules do not form during exposure equivalent to 15-20 years deployment.

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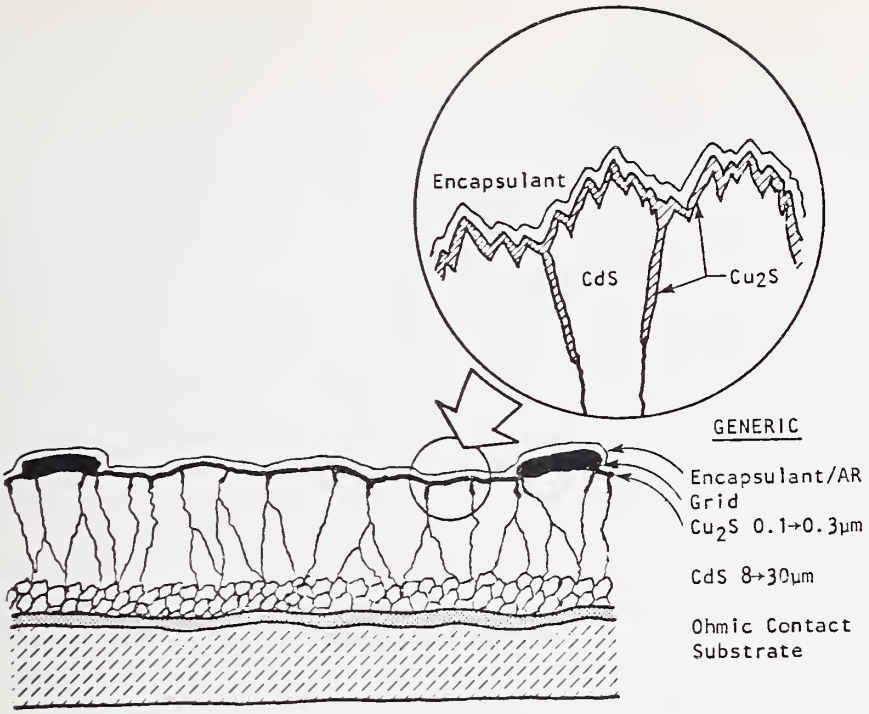

Figure 1. Cross section of a typical CdS/Cu_2S cell.

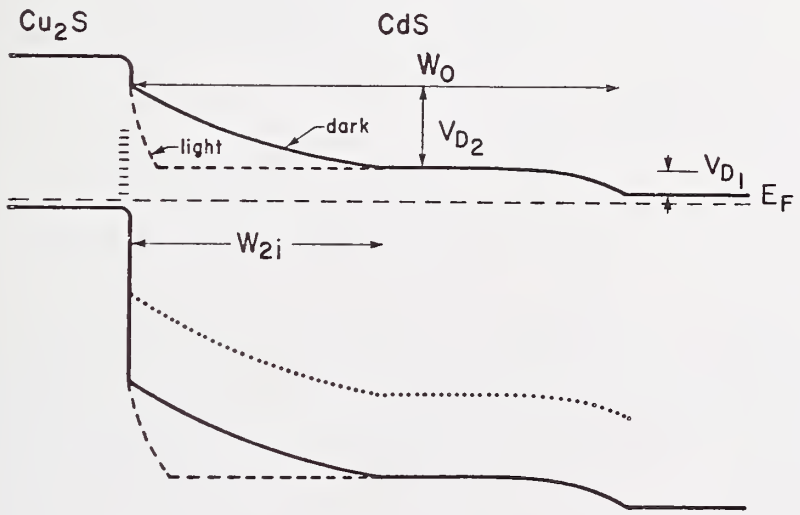

Figure 2. Band diagram for a CdS/Cu_2S cell. The conduction band discontinuity is 0.2-0.3 eV. A population of hole trapping centers lying deep in the band gap in the compensated CdS is indicated. These exist to the extent of the compensated region, W_0. W_{2i} is the width of the space charge region in the dark.

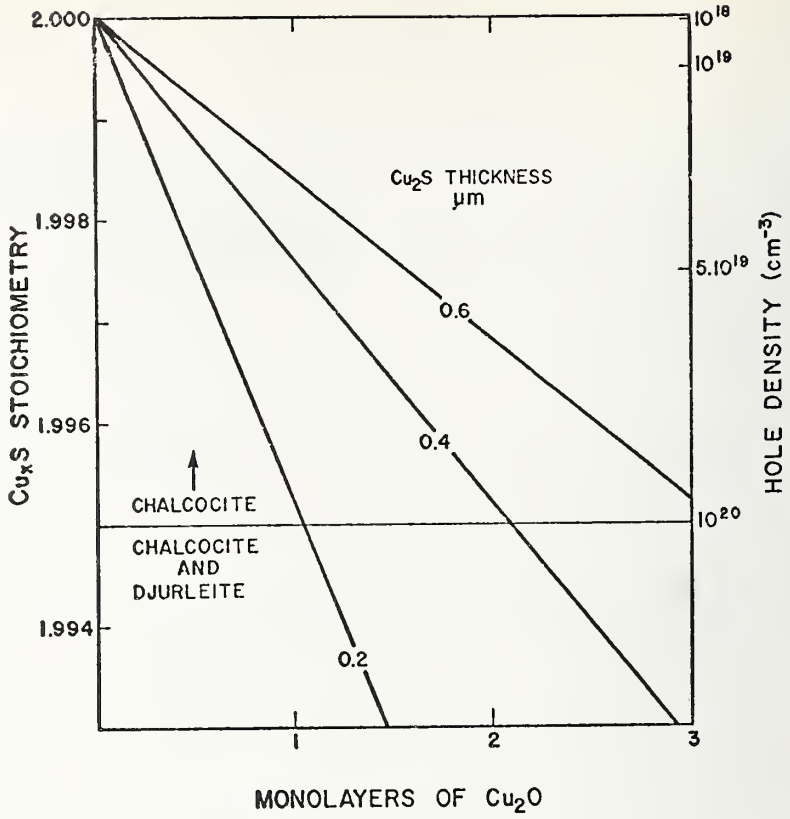

Figure 3. The influence of oxidation on the stoichiometry and hole density of initially stoichiometric chalcocite.

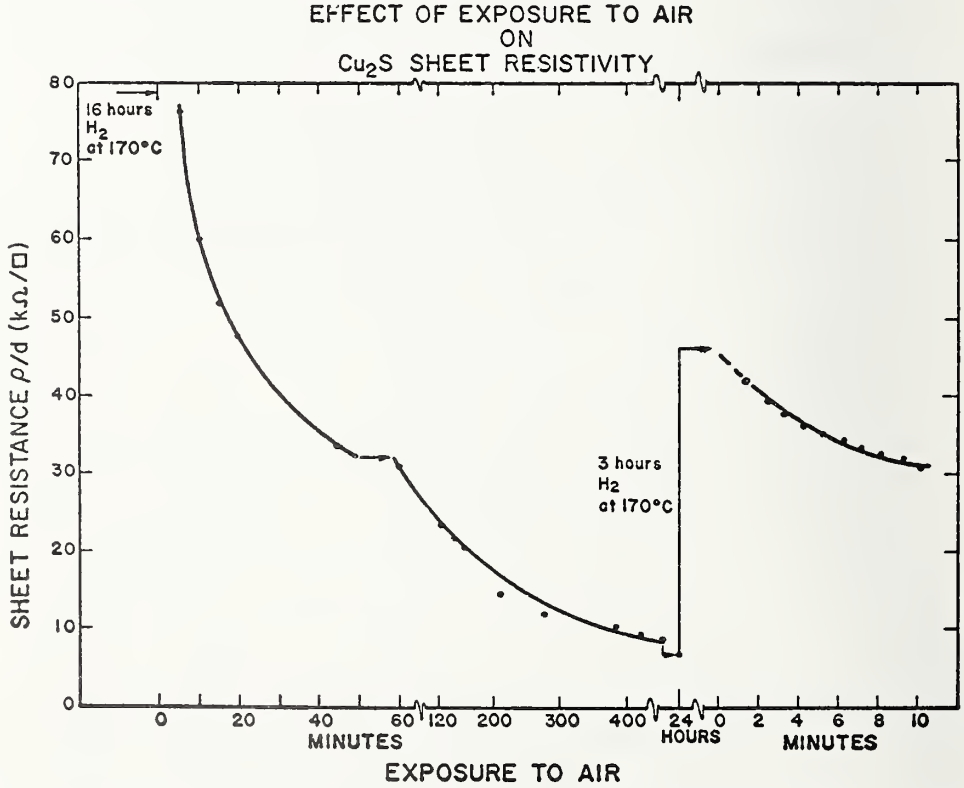

Figure 4. The reduction of Cu_2S sheet resistance on exposure to air and recovery by a reducing heat treatment.

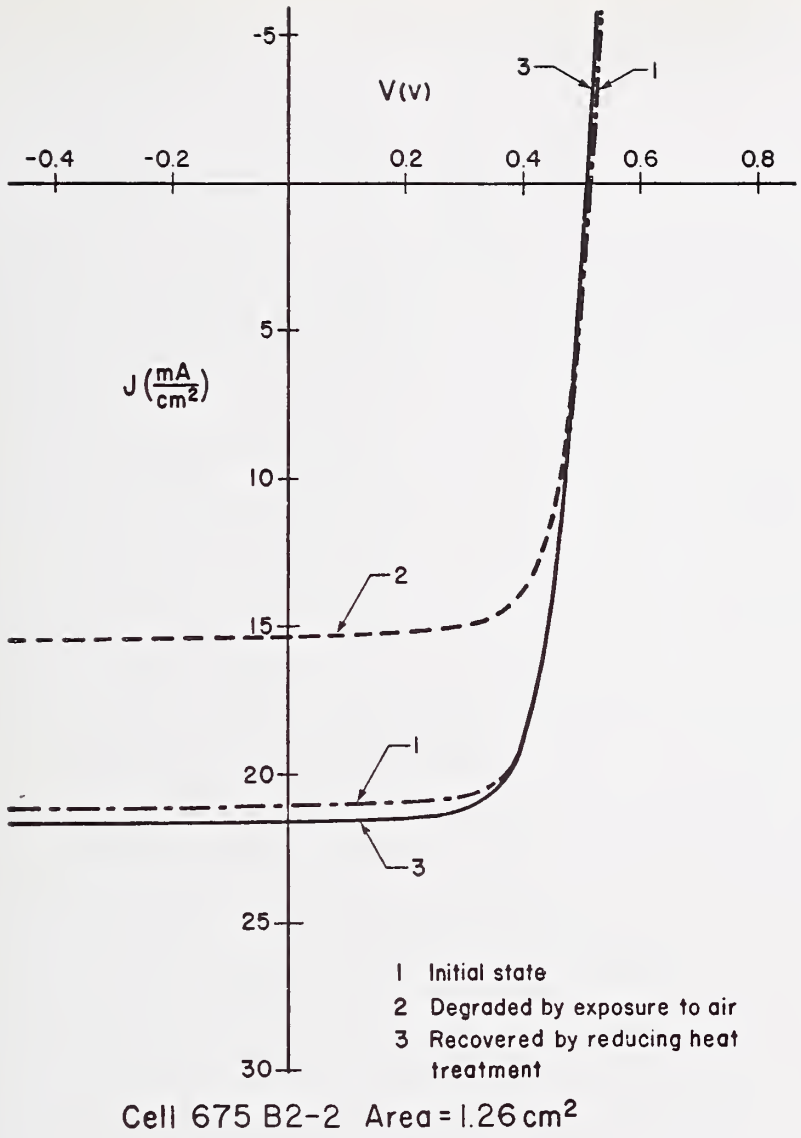

Figure 5. Loss of short circuit current on exposure to air and recovery by reducing heat treatment. The initial and final sunlight efficiency is 8.6%, the degraded state corresponds to 6.3%. Above I-V curves taken under W-I simulation.

STABILITY AND TERNARY CHALCOPYRITE PHOTOVOLTAIC DEVICES

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The photovoltaic effect in several thin-film homo- and heterodiodes using I-III-VI_2 semiconductors has been demonstrated[1-3]. The majority of this work has centered on the Cu-ternaries (i.e. $CuInS_2$, $CuInSe_2$ and $CuInTe_2$), and the success--both in demonstration and stability--has varied. $CuInS_2$ and $CuInSe_2$ thin film homojunctions, and heterojunctions of these ternaries and $CuInTe_2$ with CdS have been reported. Light J-V characteristics (under 100 mW/cm^2 illumination) of the best of these devices produced to-date are presented in Fig. 1.[3] It should be stressed that work on the Cu-ternaries--especially the thin-film photovoltaic devices--is still in its infancy. Relatively little is yet known about the device compatibility of these materials, and much good semiconductor research remains to be accomplished for them. This paper attempts to discuss the problems and stability of the Cu-ternary devices and materials based upon the experience with some laboratory, research devices.

1. STRUCTURE AND GROWTH

The Cu-ternaries used in photovoltaic devices crystallize into the chalcopyrite structure. This relatively complex arrangement is shown in the 110-projection of Fig. 2. The unit cell, indicated by the dashed lines in Fig. 2, is represented more clearly for $CuInS_2$ in Fig. 3. The chalcopyrite structure is a fairly stable arrangement for the Cu-ternaries. As an example, $CuInSe_2$ possesses this structure to 810°C, above which critical temperature a pseudocubic lattice structure results.[4] Actually in the growth of this material, crystallization into this pseudocubic modification takes place at 986°C and then transforms to the tetragonal phase at 810°C due to the ordering of the metal atoms. As might be expected for the evaporation process used to produce these ternary compounds in thin-film form, the control of the structural, electrical and optical properties is a sensitive and complex problem which depends critically on the ensemble of deposition conditions, handling and post-deposition treatments. If two layers are required (e.g. for devices), the problems multiply. To this time, a two-source deposition scheme has been necessary to control the chalcogen content, the Cu-vacancy level, and the resulting film majority carrier type. This method has produced the best device-quality layers, but better control and reproducibility is needed.

X-ray and electron diffraction data relating structural properties to deposition conditions have been reported.[5] Films have varied from multi-phased (detecting such compounds as Cu_2X and In_2X_3, where X = S, Se or Te depending on the evaporant) to good single phase material.

Recently, the presence of a semiconducting spinel ($CuIn_5S_8$) has been detected in In-rich grown "$CuInS_2$".[6] This spinel has properties similar to the chalcopyrite ternary, and only a slightly smaller bandgap. The potential for existence of this spinel exists for the other ternaries as well.

2. IMPURITY DIFFUSION AND INTERDIFFUSION

The investigations on doping the chalcopyrite-type compounds have indicated rapid changes in the electrical conductivity upon annealing and the rapid diffusion of electrically active defects.[7] Examples include the increase in resistance during the preparation of CdS heterojunctions, and the net drop in acceptor concentration at the CdS/$CuInSe_2$ interface.

Most diffusion investigations have centered on impurities in $CuInSe_2$. In single crystals, the diffusion coefficient has been found to be essentially independent of the diffusing species, whether it be Cu, Zn, Se, Cd or Ag. The rate controlling process seems to be the in or outdiffusion of Se. Tell, *et al.*[8] have reported the diffusion coefficients at 300 C for Cu, Zn and Cd (from an elemental film source) to be 1.4×10^{-8} cm^2/s into $CuInSe_2$.

The diffusion problem in the thin polycrystalline film is enhanced with a more rapid process at the grain boundary. The relatively high room-temperature diffusion coefficients reported for Cd (and other diffusants) were perceived to be potential degradation problems in the CdS/Cu-ternary heterostructures.

Fig. 4 shows a depth-compositional profile of one of the better CdS/$CuInSe_2$ devices (efficiency = 5.2%) . It was fabricated completely *in situ* and exhibits a relatively orderly change from the n-CdS to the p-ternary side. Neither the entire CdS layer, which was 4 μm thick, nor the entire $CuInSe_2$ (0.46 μm) is represented in Fig. 4 so that the junction region can be better examined. In addition to the five elements involved in the two thin films, the oxygen level was also monitored. In the *in situ* fabricated devices, no oxygen was detected either in the films or in the junction region.

A related problem which plagues the cases in which the device undergoes an external annealing (in Ar-H_2Se) after ternary deposition is shown in Fig. 5. Although relatively constant CdS and $CuInSe_2$ layers are produced and good transition of the elements from one side of the junction to the other is apparent, and oxide layer results at the interface. The source of the oxide is presumed from the inevitable exposure to atmosphere during transfer and to some oxygen in the annealing environment itself. The extent of the resulting oxide region can be limited by etching the ternary prior to the CdS deposition but it has not been eliminated completely.

The device characteristics have shown significant improvement by

annealing the solar cell for short periods (10-20 min) in 10^{-1} Pa vacuum. The indication that elemental Cd has a high diffusion coefficient in $CuInSe_2$ crystals provided some concern. Since some enhancement of the diffusion process is expected along the grain boundaries of the polycrystalline thin films and since some of these devices had shown degradation in output upon heat treatments, a study of the diffusion of the Cd from the CdS layer into the ternary thin film was initiated.

Fig. 6 shows the junction region of a device which had been annealed at 600 K for 2 hrs. This device was fabricated under the same *in situ* conditions as the one shown in Fig. 4 and had similar performance characteristics. The most apparent effect of the annealing treatment is the diffusion of the Cd into the ternary film. The S, Cu, In and Se profiles are not drastically changed. Using the Hall-Morabito formalism[10] for determing the grain boundary diffusion coefficient (using the detectability limits of AES), D' can be obtained. Fig. 7 shows D' as a function of inverse annealing temperature for diffusion of Cd from CdS into a $CuInSe_2$ thin film. The data are taken for devices which had been fabricated under the identical *in-situ* conditions, and only the post-deposition annealing temperature was changed. The grain boundary diffusion coefficient follows the relationship:

$$D' = D_o \exp(-E_a/kT) \qquad (1)$$

where $D_o = 10.6\ cm^2/s$ and $E_a = 1.5$ eV for this case.

The diffusion of Cu into the CdS is minimal and discerned in Auger data only at annealing temperature exceeding 575 K. The degradation of the Cu_2S-CdS cell is partially attributed to this mechanism. It has been proposed that the Cu-grain boundary migration problem would not be as serious in the CdS/$CuInSe_2$ cell owing to the fact that Cu is more tightly bound in the chalcopyrite lattice. These diffusion studies seem to verify this proposition.

Studies similar to those of Tell, *et al.*[8] have been performed using AES and an elemental Cd film diffusion source for both single crystal and thin film $CuInSe_2$. Fig. 7 shows the results for:

(a) Thin film, bulk diffusion within grain, elemental Cd-source:

$$D = 154 \exp(-1.25\ eV/kT)$$

(a') Thin film, grain boundary diffusion, elemental Cd-source:

$$D' = 8.4 \times 10^3 \exp(-1.15/kT)$$

(b) Single crystal, bulk diffusion, elemental Cd-source:

$$D = 160 \exp(-1.22\ eV/kT)$$

(c) Single crystal, bulk diffusion, elemental Cd-source (Tell, et al.[8])

$$D = 164 \exp(-1.19 \text{ eV}/kT)$$

For comparision:

(e) Thin film $CuInSe_2$, grain boundary diffusion, CdS source:

$$D' = 10.6 \exp(-1.5 \text{ eV}/kT)$$

Similiar data taken for $CuInS_2$ and $CuInTe_2$ reveal:

(i) Thin film $CuInS_2$, grain boundary diffusion, CdS source:

$$D' = 13.8 \exp(-1.7 \text{ eV}/kT)$$

(ii) Thin film $CuInTe_2$, grain boundary diffusion, CdS source:

$$D' = 5.05 \exp(-1.38 \text{ eV}/kT)$$

The differences between the CdS and the Cd diffusant sources are attributed to (1) the differences in concentrations and concentration gradients, (2) the stress differences at the interface, and (3) the difference in activation from each source. The agreement of the Cd-source data with that of Tell, et al.[8] is remarkable considering the difference in analysis techniques. It seems to support the proposition that the ternaries have high vacancy populations which dominate the diffusion process.

Recent absorption coefficient measurements on $CuInS_2$ thin films have detected the presence and effects of the Cu-vacancies.[9] The shoulder in the α vs photon energy characteristics (see Fig. 8) corresponds to a strong Cu-vacancy band as represented in Fig. 9.

3. SUMMARY

More work on the production and demonstation of ternary devices is necessary before a useful, systematic study can be made. The initial investigations reveal, however:

- The growth techniques and deposition parameters used in ternary film production critically affect structural and electrical properties and related device stability.
- Diffusion of many elements into crystalline regions is independent of diffusing species and the diffusion coefficient is relatively high due to vacancy population in the ternary.
- Interdiffusion along grain boundaries in the CdS/Cu-ternary devices can result in device degradation and failure especially for temperatures exceeding 500 K.

- Due to the fast diffusion of metals into the ternaries, the reliability of contacts may prove to be a problem.

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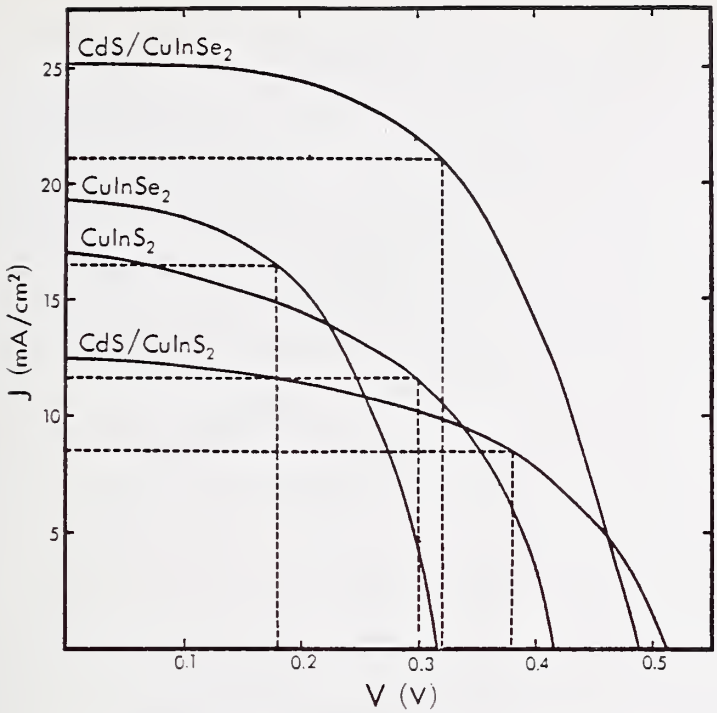


Fig. 1. Summary of J-V characteristics of Cu-ternary devices. (Illumination is 100 mW/cm^2).

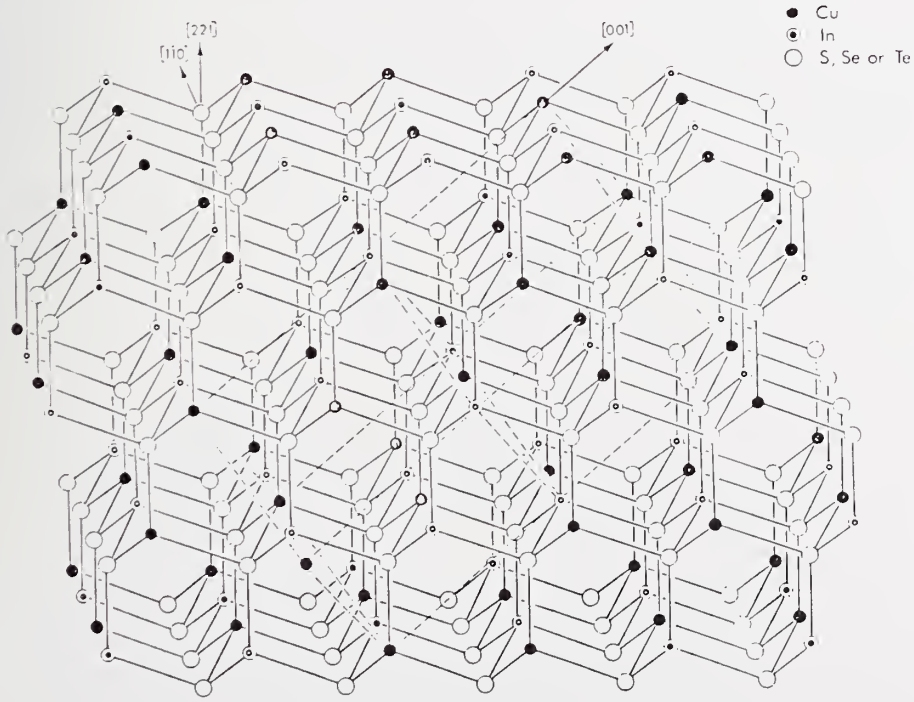
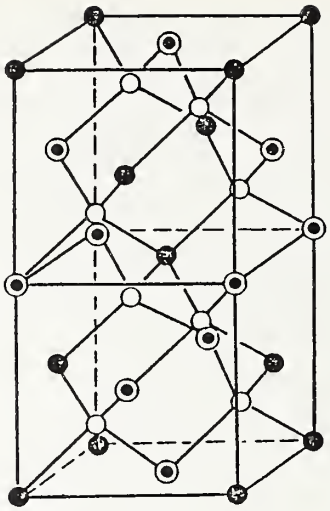


Fig. 2. 100-projection of chalcopyrite lattice. Unit cell is indicated by dashed lines.



●Cu ◉In ○S

Fig. 3. Chalcopyrite Unit Cell ($CuInS_2$).

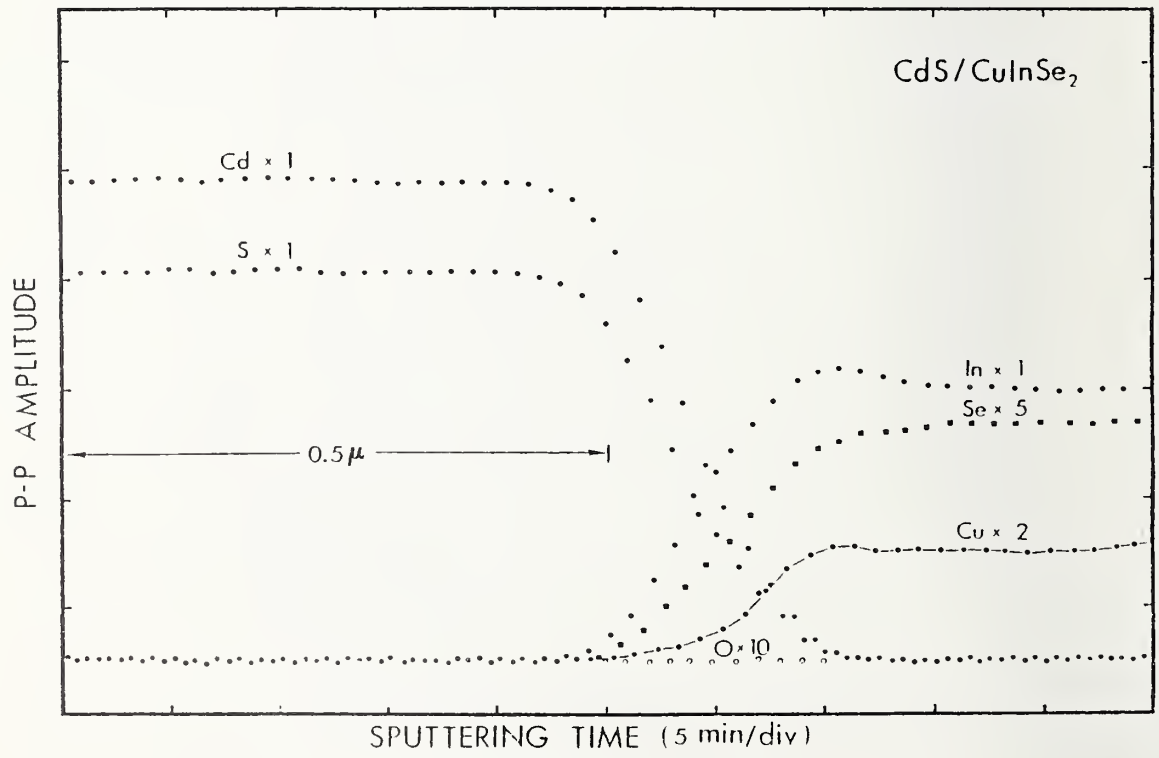


Fig. 4. Depth-compositional profile of <u>in-situ</u> produced thin-film device.

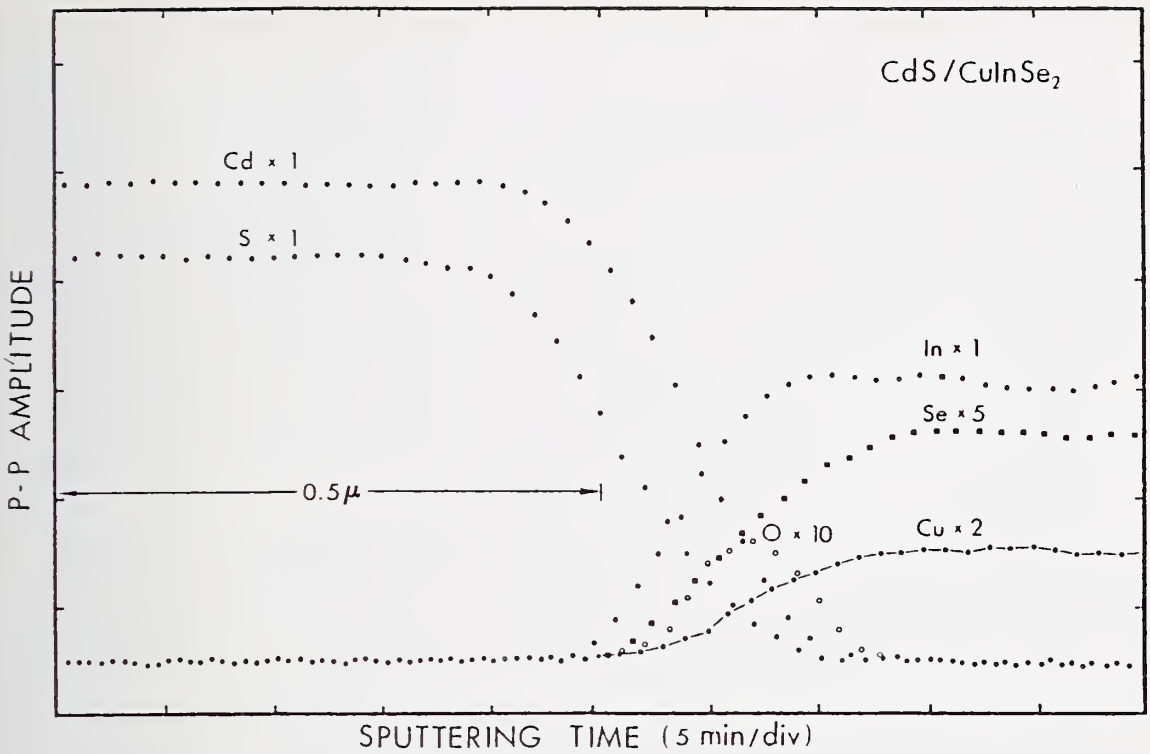


Fig. 5. AES profile of etched junction. The processing involves an external H_2Se anneal and a mild HCl etch prior to CdS deposition.

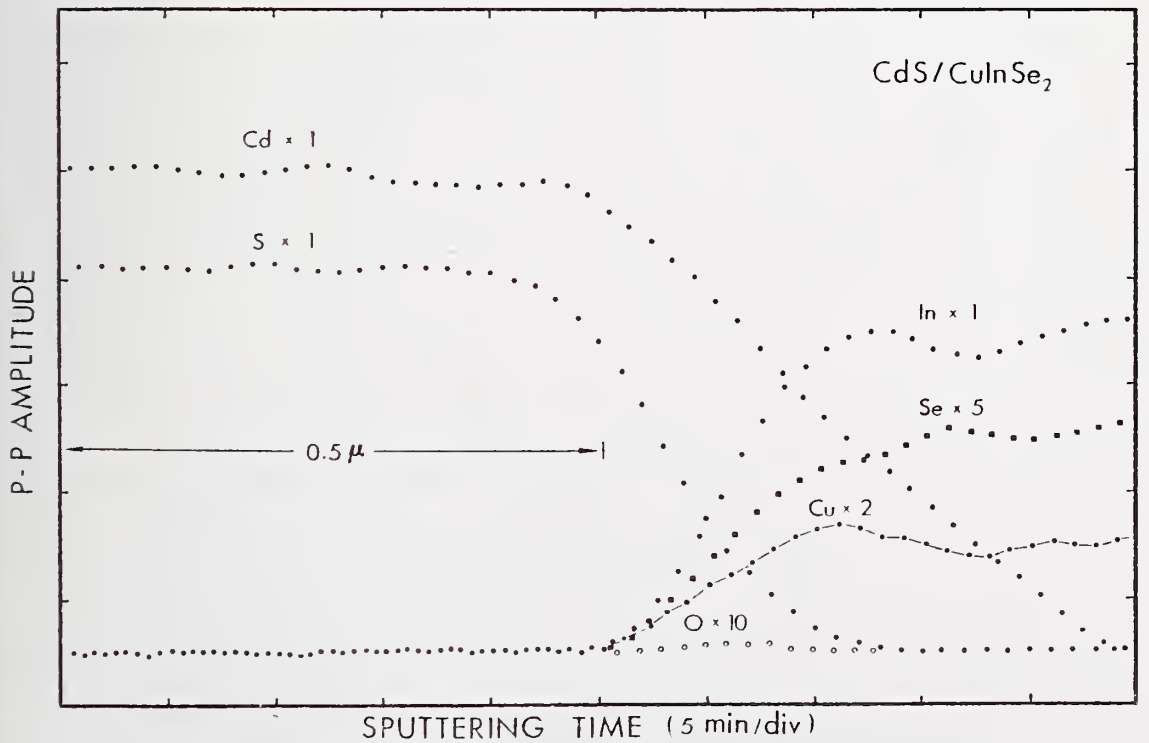


Fig. 6. Depth-compositional profile of degraded device, after annealing at 600 K, 2 hrs.

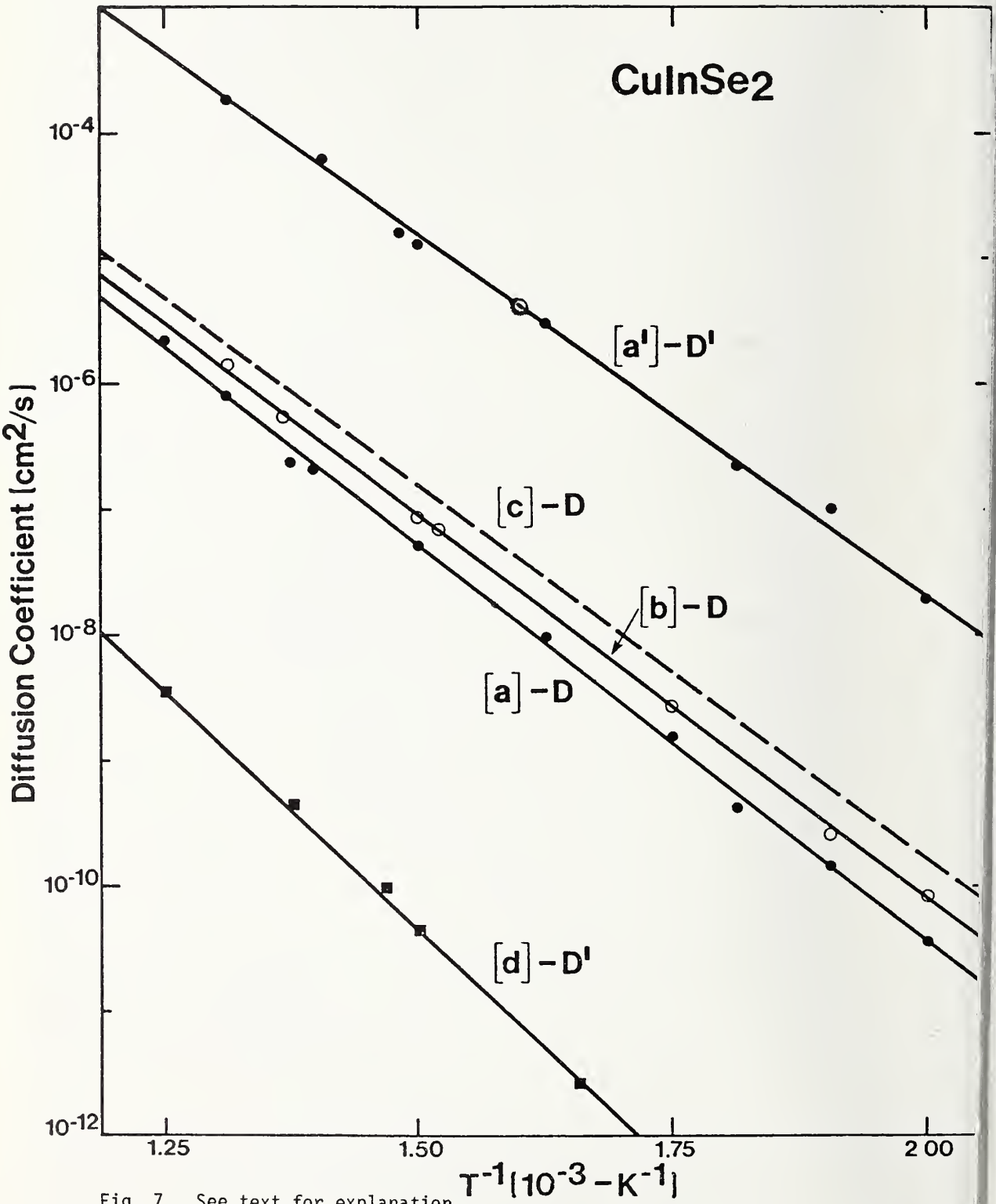


Fig. 7. See text for explanation.

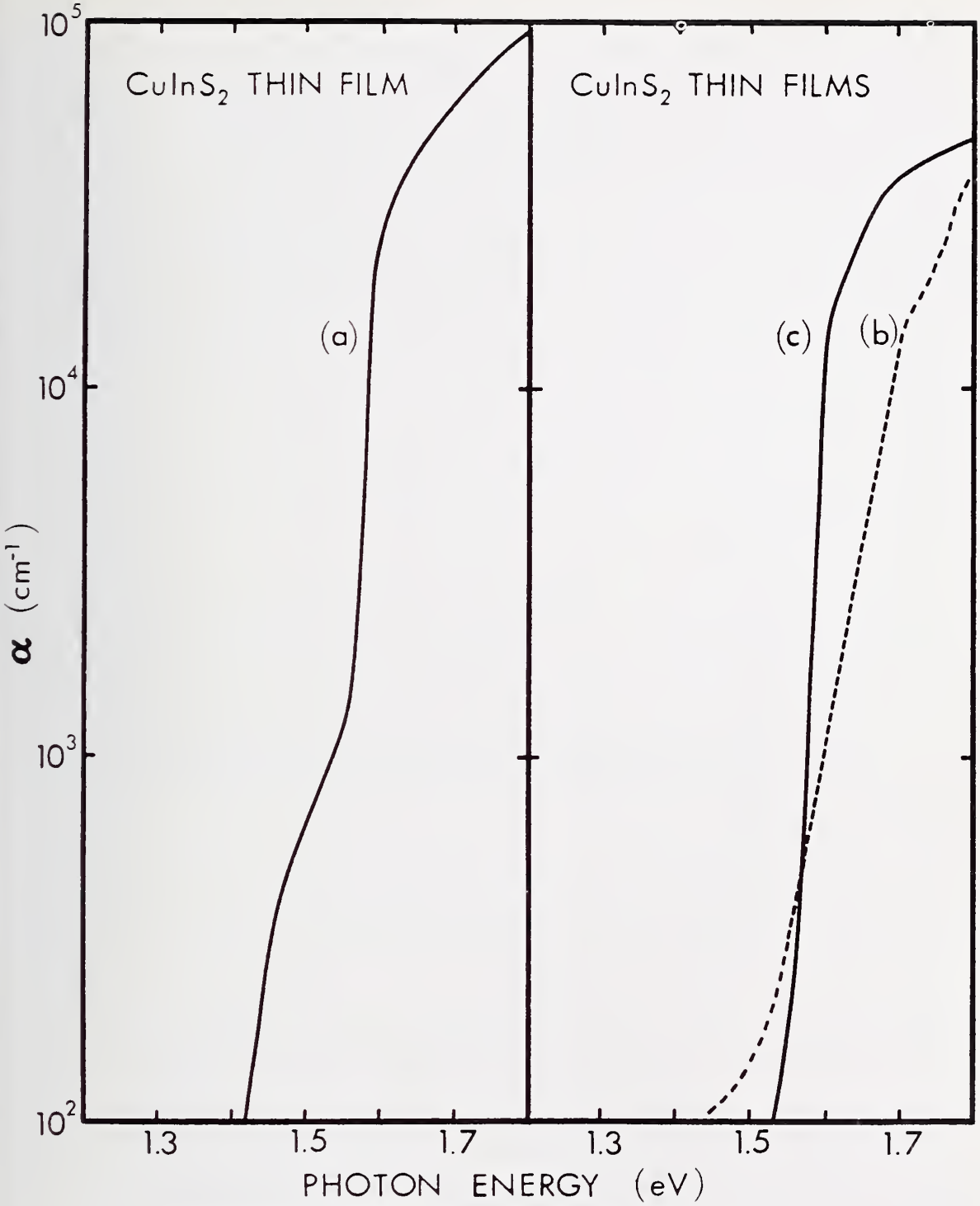


Fig. 8. Absorption coefficient dependencies of photon energy.

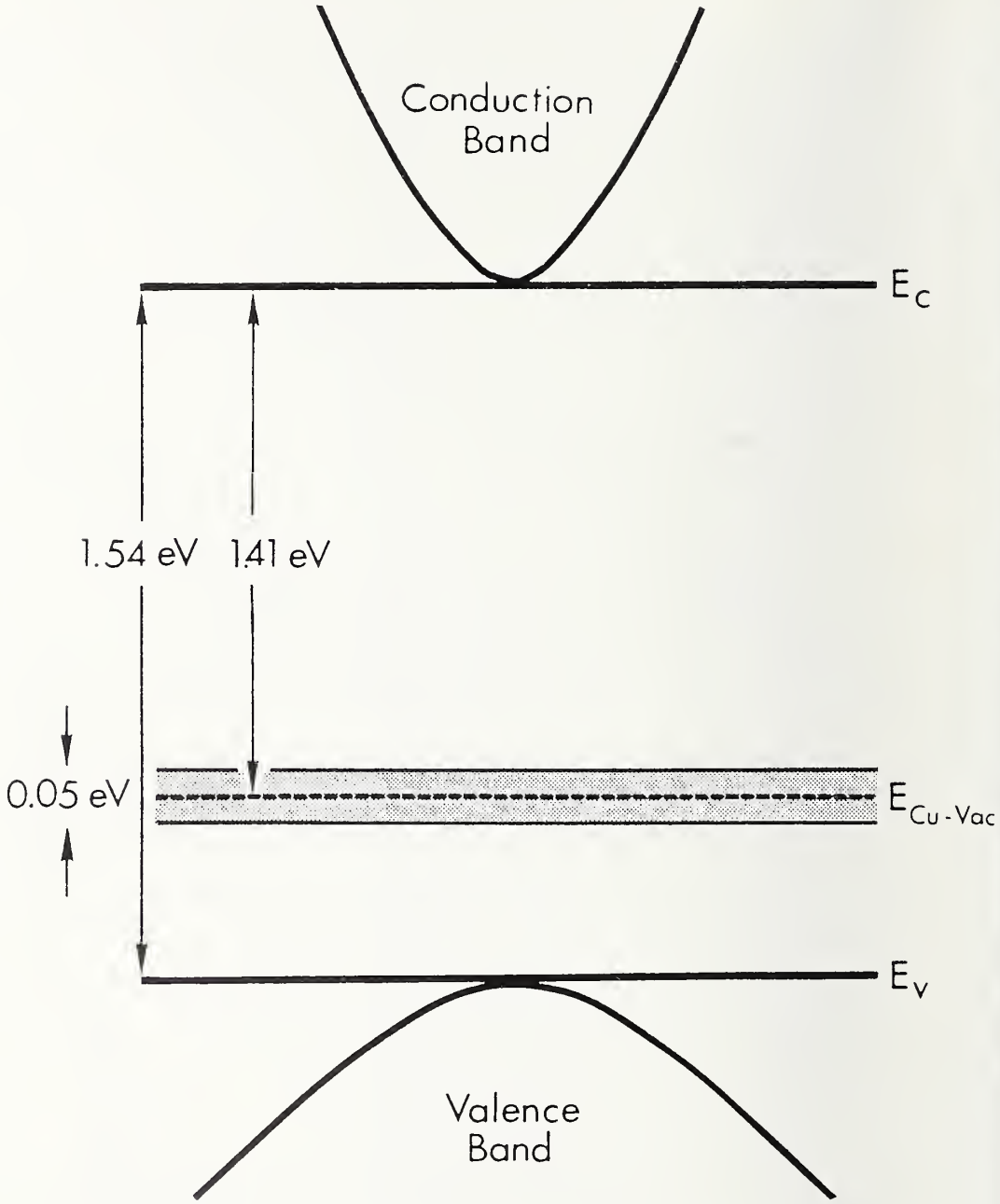


Fig. 9. Band structure representation for $CuInS_2$ thin films.

STABILITY OF THIN FILM POLYCRYSTALLINE SILICON SOLAR CELLS*

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The photovoltaic solar arrays for large scale terrestrial power generation require high conversion efficiencies, long lifetimes, and low costs. To reduce the cost of present single crystalline silicon solar cells, several approaches have been under investigation. The deposition of a thin film of silicon containing a p-n junction on a low-cost substrate appears to be a promising approach to reduce substantially the material and processing costs of single crystalline silicon cells. However, the structural and chemical properties of the silicon film are extremely important for achieving high conversion efficiencies; the concentration of grain boundaries or their effects must be minimized, and the concentration of metallic impurities must be below the tolerable levels (about $10^{15}cm^{-3}$ for some transition metals).

The thin film approach has been under investigation at Southern Methodist University during the past few years. The use of foreign substrates, such as steel and graphite, has been found to be unsuitable for the preparation of high efficiency solar cells,[1,2] due to the small crystallite size, 50 μm at best, in silicon films deposited by conventional chemical vapor deposition techniques, such as the thermal decomposition of silane or the thermal reduction of trichlorosilane. On the other hand, metallurgical silicon at a cost of about $1/kg is better suited as substrates from the structural standpoint. The use of metallurgical silicon as substrates has two major problems: high impurity content and unavailability of metallurgical silicon plates. A major portion of the metallic impurities in metallurgical silicon can be removed by chemical treatment,[3] and a unidirectional solidification technique has been developed for the recrystallization of

*Prepared for the Division of Solar Technology, Department of Energy under Contract No. EY-76-C-03-1285.

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purified metallurgical silicon on graphite for substrate purposes.[4] The active region of the solar cells can then be deposited by the thermal reduction of trichlorosilane containing appropriate dopants in a one-step process. Large area (30 cm^2) solar cells with an AM1 efficiency of 7.5% have been prepared.[5] With further process optimization, solar cells of 9-10 cm^2 area with an AM1 efficiency of 9.5% have recently been prepared. Since thin film polycrystalline silicon solar cells appear to be a viable approach for terrestrial power generation, their stabilities under temperature, humidity and optical stress have recently been under investigation. Some preliminary results are reported in this paper.

Preparation of Solar Cells

Commercial metallurgical silicon purified by chemical treatment was used for the preparation of substrates by the unidirectional solidification technique in the following manner. Metallurgical silicon was placed on a graphite plate in a fused silica tube in a hydrogen atmosphere, and graphite was heated by an rf generator. The temperature profile of the graphite plate was controlled by adjusting the spacings between the turns of the rf coil to yield a unidirectional temperature gradient of 50-80°C along the length of the specimen. The entire silicon charge was first melted, and the power was reduced for the solidification to take place from one end of the specimen to the other. This unidirectional solidification is essential because of the higher density of liquid silicon. Also, the solidification process should initiate from the surface of the melt and proceed inward to minimize the effects of random nucleations at the silicon-graphite interface. The solidified material usually consists of elongated grains up to several centimeters in length.

Since the unidirectionally recrystallized metallurgical silicon substrates are usually p-type with and electrical resistivity of 0.005 - 0.05 ohm-cm, solar cells prepared in this work were of the configuration n^+-silicon/p-silicon/metallurgical silicon/graphite. The low resistivity substrate serves to minimize the contact resistance between silicon and graphite and also provides a back-surface field. Immediately following the recrystallization of the substrate, the active region of the solar cell was deposited on the substrate at 1100°-1150°C by the thermal reduction of trichlorosilane with hydrogen, the most commonly used process for the deposition of silicon. The conductivity type and electrical resistivity of deposited silicon were controlled by using diborane or phosphine as a dopant, and the p-n junction was formed during the deposition process by varying the

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composition of the reactant mixture. Typically, 20-30 μm of 0.2 - 1 ohm-cm p-type silicon was deposited at a rate of about 1 μm/min followed by the deposition of 0.3-0.6 μm of 0.001-0.004 ohm-cm n-type silicon at a rate of about 0.1 μm/min (a graded profile was also used in some cases to provide a drift field). The deposit is usually epitaxial with respect to the substrate as shown by metallographic examinations. The sheet resistance of the n^+-layer, measured by the four point probe technique, was 30-50 ohms/square. Solar cells of the configuration p^+-silicon/n-silicon/n^+-metallurgical silicon/graphite have also been prepared, and the metallurgical silicon was doped with phosphorus prior to unidirectional solidification.

The graphite plate serves as the ohmic contact to the metallurgical silicon substrate. The grid contact of about 1000 Å of titanium and 3-5 μm of silver was evaporated onto the front surface, followed by annealing at about 525°C in a hydrogen atmosphere; 700-750 Å of tin dioxide was deposited on the cell surface at 400°C by the oxidation of tetramethyltin in an argon atmosphere. Lead wires were attached to the grid contact and the graphite substrate by means of conducting epoxy. The solar cell was then encapsulated in GE RTV 615 transparent silicone potting compound, and SS-4120 primer was used to insure strong bonding.

Characteristics of Solar Cells as a Function of Temperature

The current-voltage characteristics of thin film polycrystalline silicon solar cells were measured in the temperature range of -40° to 100°C in the dark and under illumination with ELH quartz-halogen lamps at AM1 conditions. The solar cells were of 10-30 cm^2 in area. The AM1 efficiency of 30 cm^2 area cells is usually 7 to 7.5% at room temperature. Recent process improvements have produced solar cells of 9 cm^2 area with an AM1 efficiency of 9.5% at room temperature. Figure 1A shows the room temperature current voltage characteristics of a solar cell of 30.8 cm^2 in area under AM1 illumination, where the open-circuit voltage, short-circuit current density, and fill factor are 0.56V, 20 mA/cm^2, and 67%, respectively, corresponding to a conversion efficiency of 7.5%. Figure 1B shows the characteristics of a solar cell of 9 cm^2 in area, and its AM1 efficiency is about 9.5% at room temperature.

The variation of open-circuit voltage, short-circuit current density, fill factor and AM1 efficiency of the solar cell in Figure 1A is shown in Figure 2. The open-circuit voltage, fill factor, and conversion efficiency all decreased with increasing temperature while the short-circuit current density increased with increasing temperature, as expected. The open-circuit voltage decreased from 730 mV at -40°C to 350 mV at 103°C, and this variation is essentially linear with a slope of -2.8 mV/°C, as compared with about -2 mV/°C for single crystalline silicon solar cells.(6) The short-circuit current density also varies

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[6] J. D. Sandstrom, in Conference Record of the 6th IEEE Photovoltaic Specialists Conference, March 1967, p. 199.

linearly with temperature at a slope of about 0.034 mA/cm^2°C, very similar to the temperature coefficient of single crystalline silicon solar cells.[6] The fill factor of the solar cell was found to decrease from 70% at -40°C to 53% at 103°C. Its AM1 efficiency decreased from 9.5% at -40°C to 4.3% at 103°C, and the rate of decrease is about 0.036%/°C. The characteristics of the solar cell remain unchanged after temperature cycling between -40°C and 100°C. These results indicate that the performance of polycrystalline silicon solar cells on graphite compares favorably with that of single crystalline silicon solar cells with regard to the dependence of device parameters on temperature.

At temperatures of -150°C or below, solar cells fractured due presumably to dissimilar thermal expansion coefficients of the silicon and the RTV-615 encapsulant. Cell destruction occurred within the polycrystalline silicon rather than at the graphite-silicon interface, indicating the strong bonding between graphite and silicon.

Thermal Stress

Several solar cells were heated at 115°C for up to 160 hours, and no change in characteristics was observed. They were also subjected to temperature cycling between -40°C and +100°C; the heating and cooling were carried out at a rate of about 7°C/min, and the cell was maintained at the desired temperature for one hour. The results of a typical test are shown in Table I, where no degradation was observed after 20 cycles.

Table I Effects of temperature cycling on characteristics of a solar cell.

No. of Cycles	V_{oc}(V)	I_{sc}(mA)	FF*
0	0.54	406	0.65
9	0.545	410	0.60
15	0.545	410	0.62
20	0.545	410	0.65

Effects of Humidity

To determine their stability under high humidity conditions, thin film silicon solar cells were placed in a reflex apparatus containing boiling deionized water. The humidity was then effectively 100% with condensation of water occuring on solar cells and condenser walls and draining back into the reflux reservoir. The results of a typical test are shown in Table II; some apparent variations in cell parameters may be associated with water absorption and desorption by RTV. The characteristics were generally measured several hours after the cells were removed from the reflux apparatus.

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*fill factor

Table II Effects of humidity on characteristics of a solar cell.

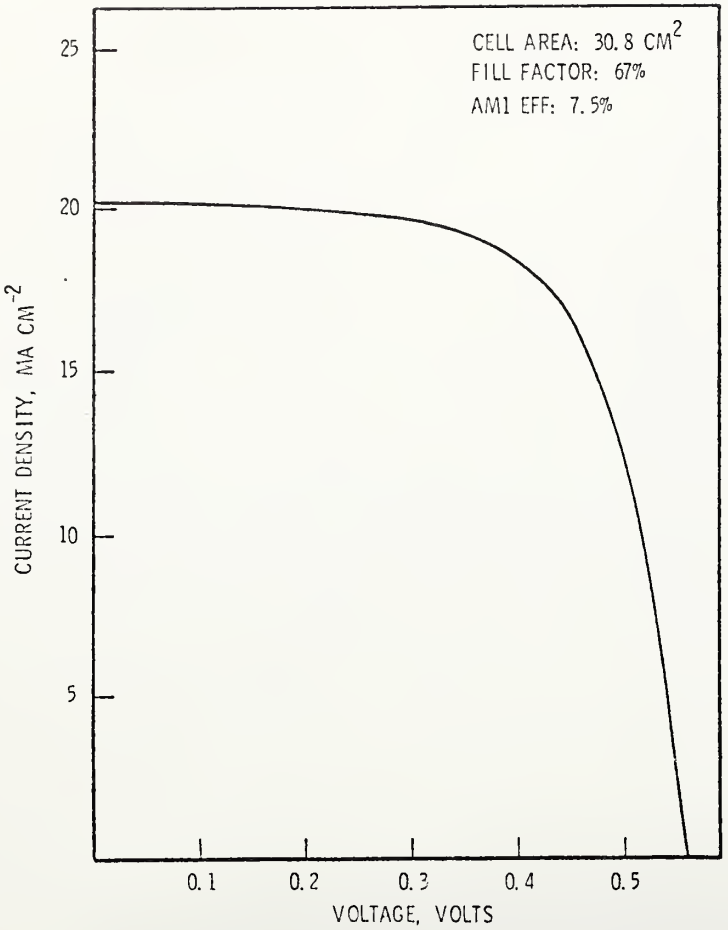
Time(h)	V_{oc}(V)	I_{sc}(mA)	FF
0	0.544	414	0.63
6	0.55	419	0.60
12	0.543	410	0.64
16	0.543	414	0.63

Optical Stress

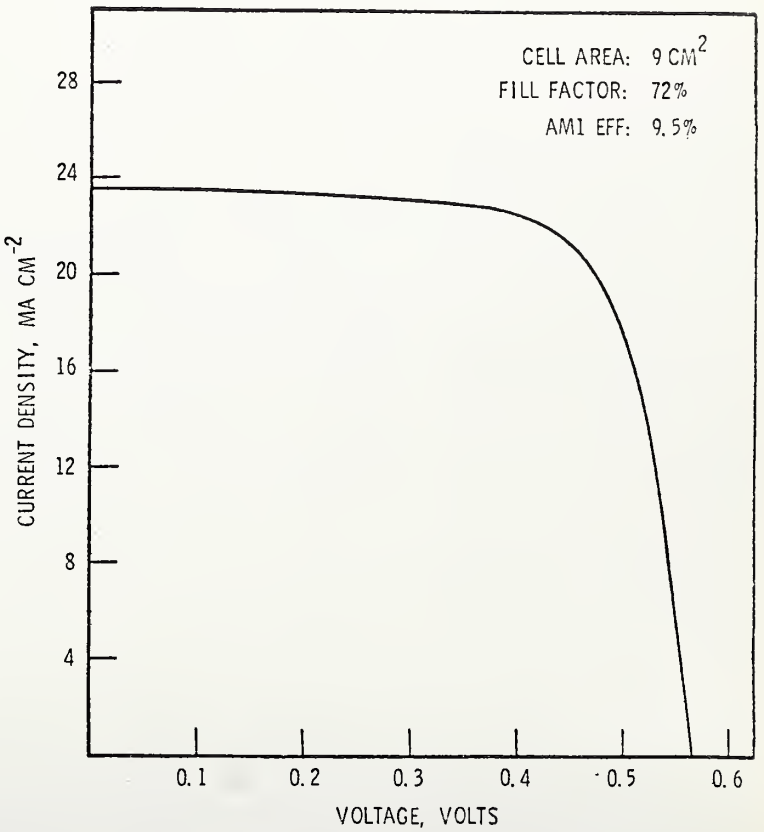
A solar cell was illuminated under a power density of 1.2 W/cm^2 at 150°C with a 0.2 ohm load for 150 hours. Some degradation in cell characteristics was observed due presumably to the deterioration of the grid contact. The open-circuit voltage, short-circuit current, and fill factor were 0.562V, 620 mA, and 71%, respectively before testing, and were 0.55V, 605 mA, and 62%, respectively, after testing.

Summary and Conclusions

Thin film polycrystalline silicon solar cells have been prepared by the deposition of a silicon film containing a p-n junction on a metallurgical silicon substrate. The temperature coefficients of parameters of thin film solar cells compare favorably with those of single crystalline silicon solar cells. The thin film solar cells are stable under thermal stress and high humidity conditions indicating that they are promising for terrestrial applications.



(A)



(B)

Figure 1 Current-voltage characteristics of two solar cells under illumination with ELH quartz halogen lamps equivalent to AM1 conditions.

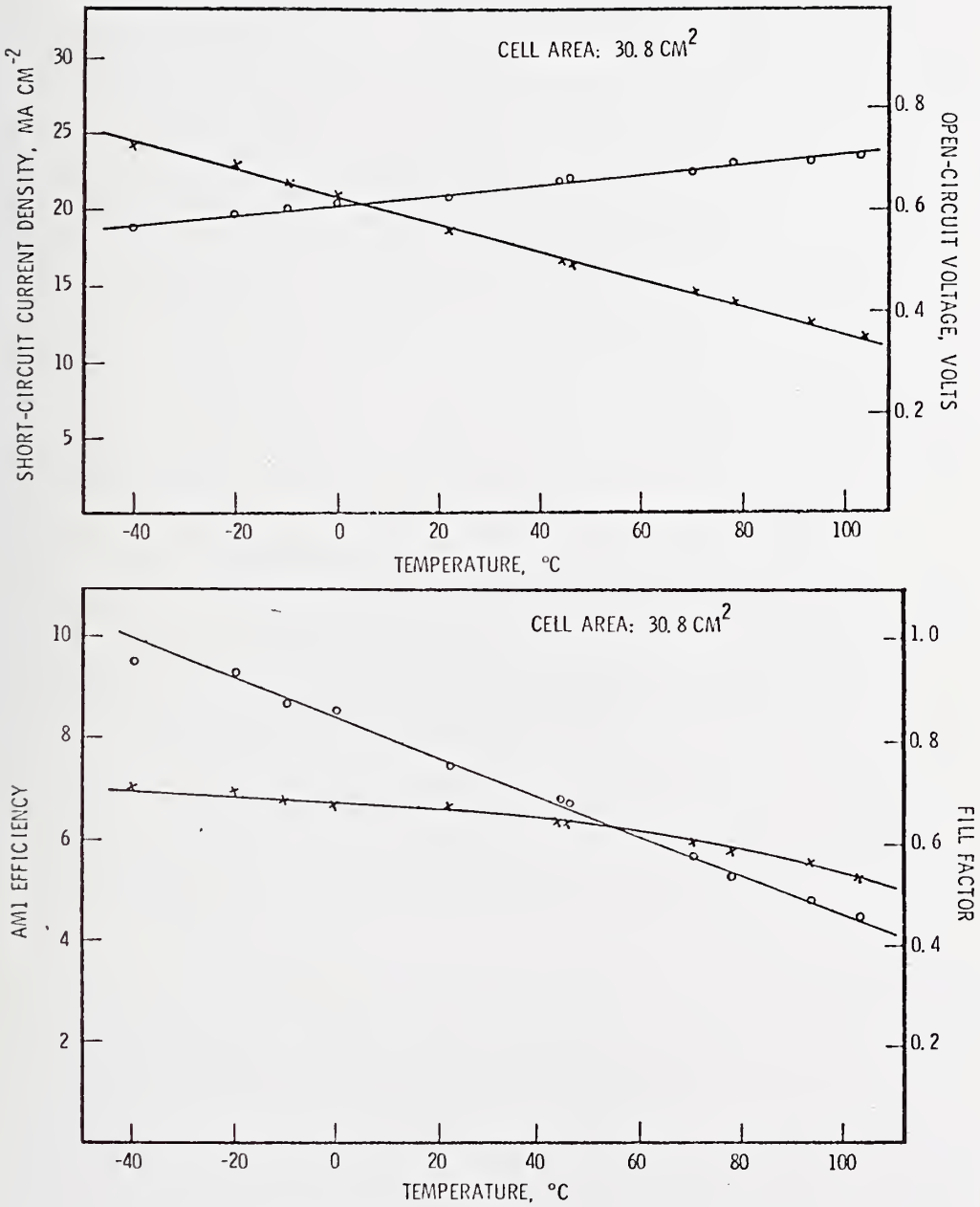


Figure 2 Characteristics of a large area thin film polycrystalline silicon solar cell as a function of temperature.

RELIABILITY STUDIES ON MIS AND TRANSPARENT OXIDE-Si SOLAR CELLS*

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INTRODUCTION

MIS solar cells having a Cr/oxide/p-type silicon structure are being studied for use in terrestrial solar energy conversion. More details of a typical structure are shown in Figure 1 where the oxide gives increased open circuit voltage (V_{OC}), the Cu decreases sheet resistance to improve fill factor (F) and the A/R coating increases current density (J_{SC}). This structure has produced 2 cm^2 cells having

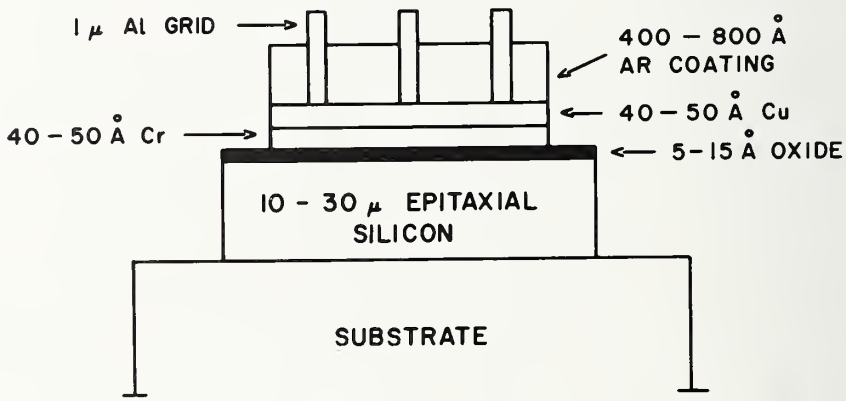

Figure 1. Diagram of a Schottky MIS solar cell

*Research supported by the NSF-RANN Program with technical supervision by the Department of Energy

12.2% efficiency on Monsanto single crystal silicon and 8.8% efficiency on Wacker polycrystalline silicon. The MIS structure is promising for developing an economical and continuous fabrication process using thin silicon on a low-cost substrate.

The data reported herein involve results of preliminary studies concerning reliability and degradation of MIS solar cells. A review of data supplied by other researchers in the field and past data on the Cr/oxide/Si system is first given. More recent data on the Cr/oxide/Si system are then presented including environmental studies and Auger analysis. The object of this study is to give direction to future work on MIS devices involving questions of stability, bonding, and encapsulation. Hopefully, a MIS cell can be fabricated which gives a 20 year life with little degradation.

A similar structure exists by replacing the A/R coating and metal by a metal oxide such as SnO_2 to form a heterojunction solar cell having a transparent window. This structure is beneficial from the standpoint of increased optical transmittance into the silicon. This paper also summarizes the results reported by R. L. Anderson of Syracuse University concerning degradation effects when using window materials of SnO_2, In_2O_3, and indium-tin oxide.

Previously Identified Degradation Effects in MIS Solar Cells

Very few results have been previously reported concerning degradation effects on MIS solar cells using silicon. Some preliminary work by Kipperman[1] on Au-p-type silicon devices having an oxi-fluorite insulator and no A/R coating have been reported. He obtained a V_{oc} decrease by 15%, after a temperature soak at 50°C for 4 hours, which may be caused by a fluorine release to influence trap density. An initial 15% increase in J_{sc} was attributed to reduced reflection caused by changes in the Au layer. A further treatment at 100°C for 4 hours caused a 20% reduction in V_{oc} and also a significant degradation in fill factor as shown in Figure 2. These cells were by no means optimized but were designed to study the oxi-fluorite layer.

An analysis of a Au-n-type Si Schottky solar cell by Pananakakis, Viktrorovitch, and Ponpon[2] was made to study the effect of oxide growth on the barrier formation. After fabrication and upon exposure to air it was found that the I-V characteristics would change with time. An initial increase in V_{oc} from 0.0V to 0.19V was seen for 120 minutes air exposure on a device having a 300 Å Au layer. Further exposure to air caused a decrease in fill factor from about 0.68 to 0.25 and a decrease in J_{sc} by a factor of four as shown in Figure 3. The initial

[1] A. H. M. Kipperman, private communication.

[2] G. Pananakakis, et al., Revue du Physique Applique, to be published.

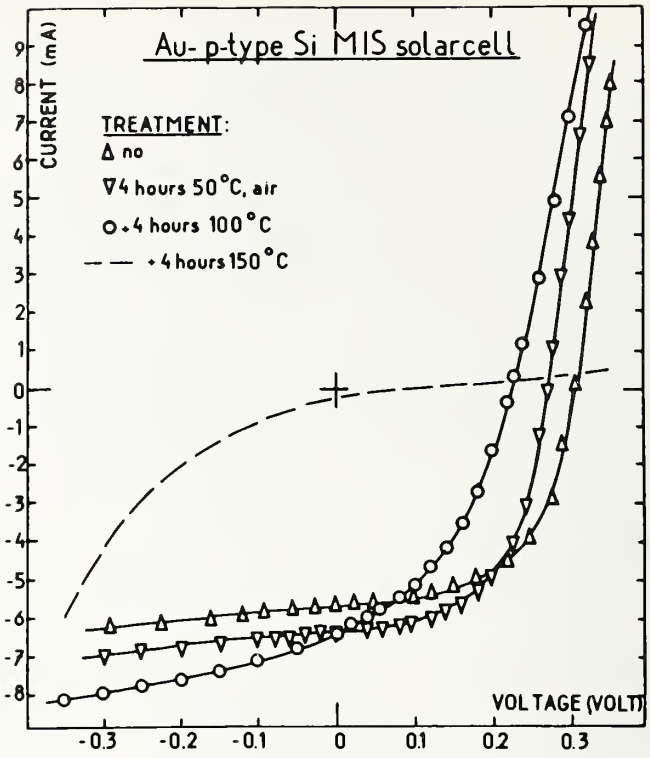

Figure 2. Degradation in Au-p-type Si MIS solar cell due to degradation of the oxi-fluorite insulator [REF. 1]

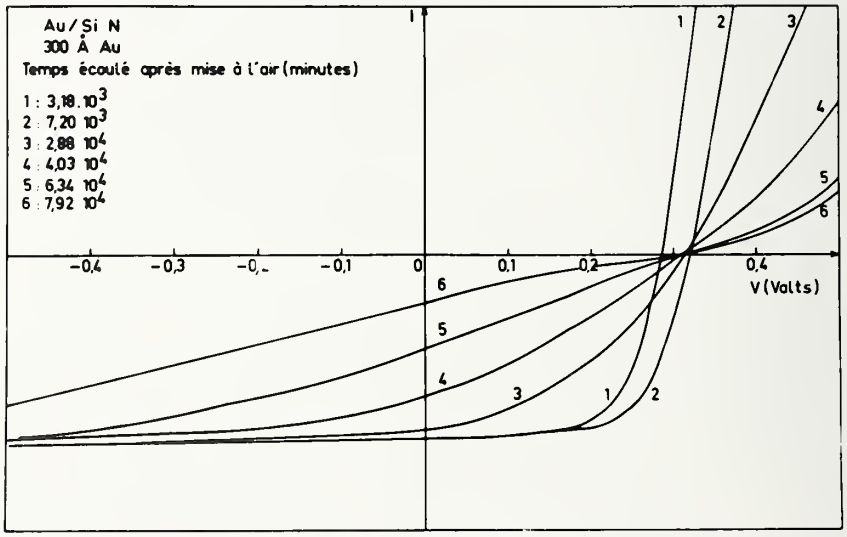

Figure 3. Degradation in Au-n-type Si MIS solar cell due to excess thickness of interfacial oxide [REF. 2]

improvement in V_{oc} is attributed to an initial growth of thin oxide to an optimum thickness which forms a MIS device. Further exposure to air gave an oxide thickness in excess of the optimum value to reduce fill factor and J_{sc}.

A further study has been conducted by Townsend[3] on Al-p-type Si MIS solar cells. A slow Al deposition was critical to produce an Al film which did not degrade with prolonged exposure to air. One observation involved a MIS cell oxidized in air at 400°C to form a 19 Å oxide prior to Al deposition. Five days of prolonged air exposure after fabrication caused a significant decrease in V_{oc} and fill factor. This was attributed to water vapor trapped within the oxide during oxidation which later caused the formation of an aluminum oxide interface in addition to the grown silicon oxide layer. Cells annealed in H_2 or oxidized in dry O_2 did not show this degradation behavior. Properly fabricated cells did show an initial 10% decrease in V_{oc} accompanied by an increased J_{sc} to preserve the efficiency but then exhibited stable characteristics. Some cells have shown a continued decrease in V_{oc} with time but were restored by a simple heat treatment.

Our previous research in this area[4] compared 50 Å Cu/40 Å Cr/20 Å oxide/Si to 50 Å Ag/40 Å Cr/20 Å oxide/Si using electronic and Auger analysis. A comparison was made between Cu/Cr/oxide/Si, heated Cu/Cr/oxide/Si, and Ag/Cr/oxide/Si. Inferior electrical characteristics were observed for the Ag/Cr system. The Ag/Cr system also was not as stable in that Auger analysis detected the penetration of Ag through the Cr to the silicon which then reduced the barrier height and V_{oc}. The heated Cu/Cr system gave data identical to the non-heated Cu/Cr. Several cells were non-hermetically encapsulated in Sylgard 184 or polystyrene cases. Polystyrene gave more stable performance during 1-2 years of environmental testing. This was due in part to the fact that polystyrene did not contact the cells whereas the Sylgard 184 did make intimate contact with the cells. A hermetic seal was recommended for more stable performance with time.

Recent Experimental Observations on Cr-oxide-Si Solar Cells

Data are now available on several other reliability studies performed on the Cr/oxide/Si MIS solar cell. Most cells had a SiO antireflection coating. Current leads were bonded to the cells using a silver-epoxy conductive cement. The cells were then potted in Sylgard 184 or placed in epoxy sealed polystyrene cases. Each cell was tested in the laboratory, placed on the roof for continuous operation at the maximum power point, and then tested monthly in the laboratory to establish a record of changes in performance. Table 1 contains a summary of data collected on three different solar cells. Cell 226 was of Cr/Cu/Cr/oxide/Si structure encapsulated in Polystyrene. It has shown a slight initial degradation in V_{oc} and a slight decrease in F over a 2 year period. A slight change in contact resistance could be a partial cause for these observations. Cell 239 was constructed using Cr/Ag/Cr/oxide/Si with a Sylgard encapsulant. A

[3] W. G. Townsend, private communication; W. C. Townsend and D. R. Lillington, Proc. 1977 Photovoltaic Solar Energy Conf., Luxembourg, 27-30, Sept. 1977, pp. 207-213.

[4] J. K. Kim, et al., J. Elec. Mtls., accepted for publication.

TABLE 1

A Summary of Photovoltaic Data for Schottky Solar Cells Exposed to Environmental Testing

Sample	Date	V_{oc} (V)	I_{sc} (mA)	F	T (°C)	Structure	Encapsulation
226	4/30/76	0.51	28	0.64	-	Cr-Cu-Cr	Polystyrene
	4/7/77	0.48	24	0.65	23		
	9/23/77	0.46	26	0.63	24		
	2/9/78	0.47	26	0.61	26		
239	4/30/76	0.55	38	0.61	-	Cr-Ag-Cr	Sylgard
	4/7/77	0.53	30	0.50	23		
	9/23/77	0.52	30	0.50	24		
	2/9/78	0.52	28	0.54	26		
272	9/29/76	0.52	14	0.63	23	Cr-Cu-Cr No AR coating	Polystyrene
	4/7/77	0.53	12	0.60	23		
	9/23/77	0.52	12	0.60	24		
	2/9/78*	0.50	12	0.30	26		

*A visible crack appeared in the cell caused by improper mounting

significant decrease in I_{sc} is caused by discoloration of the encapsulant. 10% decrease in F may be caused by diffusion of the Ag metal observed in previous research[4]. Table 1 also contains data for a Cr/Cu/Cr/oxide/Si cell 272 which did not have an A/R coating to permit future Auger analysis. This cell was quite stable until a crack developed due to improper mounting. An extensive analysis of this cell was made as reported in the following paragraphs.

Dark I-V data on cell 272 were obtained before and after environmental testing. These data are almost identical even after 1 1/2 years of continuous operation in the environment where temperature extremes of -20°C to +100°C have been found. The slight decrease in slope at high voltages for the curve after environmental testing may be caused by increased solar cell resistance due to the crack. Results of analyzing the photovoltaic data and dark I-V curves are given in Table 2. The ideality factor (n) and barrier height (ϕ_B) were calculated from the dark I-V curves at voltages >0.4 V. The change in V_{oc} from these factors can be calculated using the equation [5]

$$V_{oc} = n\left(\frac{kT}{q}\right)\left[\ln\left(\frac{J_{sc}}{J_o}\right) + X^{1/2}\delta\right] \qquad (1)$$

TABLE 2

Electronic Data Taken at Intervals During
Environmental Testing of MIS Solar Cell 272

When Tested	V_{oc}* (V)	J_{sc}* (mA)	Fill Factor	n**	ϕ_B** (eV)
7/19/76	0.53	12	0.76	1.73	0.83
4/7/77	0.53	12	0.60	-	-
9/23/77	0.52	12	0.60	-	-
2/9/78***	0.50	12	0.30	2.27	0.77

* Measured using 100 mW/cm^2 simulated sunlight
** Calculated from dark I-V curve for V>0.4 volts
*** A visible crack has appeared in the solar cell

and

$$J_o = A^*T^2 \exp\left(\frac{-q\phi_B}{kT}\right) \tag{2}$$

with $X^{1/2}\delta$ = tunneling coefficient, and A* = Richardson's constant. These equations may be combined to obtain the equation

$$V_{oc} = n\phi_B + n\frac{kT}{q}\left[\ln(J_{sc}) - \ln(A^*T^2) + X^{1/2}\delta\right] \tag{3}$$

Equation 3 is further reduced to

$$V_{oc} = n(\phi_B - 0.481) \tag{4}$$

using J_{sc} = 10 mA/cm^2, and $X^{1/2}\delta = 1$[5]. Under illumination, Card[5] has found n to reduce by 20% and ϕ_B by 2% when the effective δ < 20 Å. We have found experimentally that n increases by 9% to n' and ϕ_B decreases by 7% to ϕ_B' during solar cell illumination. This trend in n and ϕ_B is predicted by[6]

$$\phi_B = \frac{0.85}{n} + 0.30 \tag{5}$$

These differences in behavior can be attributed to differences in the MIS structures in this work and that reported by Card. Thus using equation 4 and data from Table 2, n = 1.73 and ϕ_B = 0.83 eV give n' = 1.88 and ϕ_B' = 0.772 eV to predict V_{oc} = 0.55 V which is close to the value in Table 2. After environmental testing, n = 2.27 and ϕ_B = 0.77 eV give n' = 2.47,

[5] H. C. Card, Solid-State Elec., 20, pp. 971-976, 1977.
[6] W. A. Anderson, et al., IEEE Trans. Elec. Dev., 24, pp. 453-457, 1977.

$\phi_B' = 0.716$ and $V_{oc} = 0.51$ V after $X^{1/2}\delta$ is set ≈ 0. The reduced value of $X^{1/2}\delta$ can occur by a reduction in the effective δ and a change in the oxide properties caused by penetration of the Cr during environmental testing. An increase in series resistance should not decrease V_{oc} but would account for the decreased F.

An Auger profile on a MIS cell having the structure 50 Å Cr/50 Å Cu/40 Å Cr/oxide/Si is shown in Figure 4. This profile has been repeated on several samples and does represent typical MIS structures after fabrication. It is important to observe that Cu does not penetrate the Cr to disturb the oxide-Si interface. An Auger profile was also taken on cell 272 after the extended environmental study. This profile is given in Figure 5 where a structure of 8 Å Cr/67 Å Cu/46 Å Cr/20 Å oxide/Si was used. The profile is quite similar to that of Figure 4 (disregarding differences in metal thickness) indicating that no severe changes occurred during environmental testing. An examination of the region at the Si interface is of greatest interest when considering changes in V_{oc}.

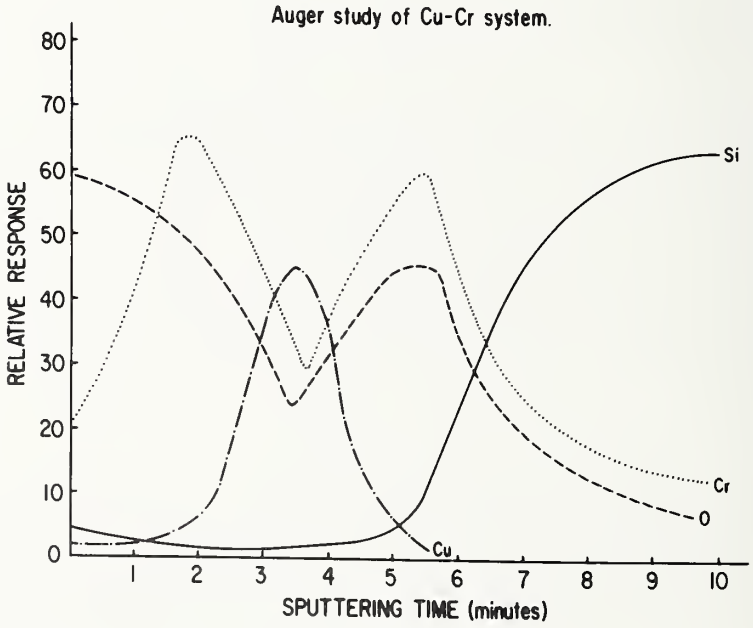

Figure 4. Auger study of a Cu-Cr system prior to environmental study

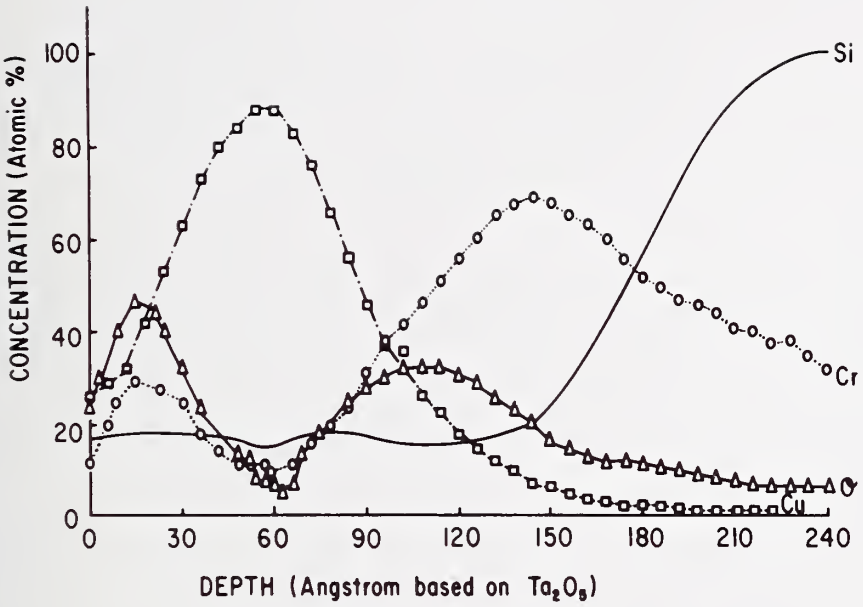

Figure 5. Auger study of a Cu-Cr system after environmental testing

Cu is at the 5% level when the Si begins to increase which is the same in Figure 4. This suggests that Cu diffusion is not a major problem. The Cr peak is wider in Figure 5 with a contribution in the Si region at the 30% level when the Si curve becomes flat. This is somewhat higher than the data shown in Figure 4 and suggests the diffusion of Cr during these environmental tests. The shape of the Cr profile near the Si region in Figure 5 does not exhibit the high rate of decay (somewhat exponential in shape) shown by all other curves in this region (Cu in Figure 5; Cu, O, and Cr in Figure 4). This also indicates the diffusion of Cr to alter the expected profile.

Degradation effects in Metal Oxide/Si Heterojunction Solar Cells

SnO_2/Si cells have shown a significant degradation evidenced by increased resistance, decreased fill factor, and variation in V_{oc}[7,8]. Degradation appears to be caused by formation of an SiO_2 layer between the SnO_2 and Si due to field assisted transport of O_2^- from the SnO_2 to the Si.

[7] T. R. Nash and R. L. Anderson, IEEE Trans. Elec. Dev., 24, pp. 468-472, April 1977.

[8] R. L. Anderson, NSF Report #NSF/RANN/SE/AER76-04168/PR/77/3,4, January 1977.

The effect is enhanced in n-Si substrates and diminished in p-Si substrates due to changes in electric field direction. A similar effect is seen in indium tin oxide/Si structures in which O_2^- migration causes the growth of an excess SiO_2 layer.

In_2O_3/Si cells have been found to degrade for temperatures in excess of 300°C. SiO_2 formation again reduces the quality of performance as reported above. Contact degradation has also been observed. The use of Al contacts can lead to the formation of Al_2O_3.

Conclusions

An evaluation of data from other researchers suggests several important factors concerning MIS solar cells. Moisture must be avoided to prevent degradation at the oxide-Si interface. Any insulator except for SiO_2 must be carefully studied to evaluate long-term stability. Deposition rates of the various metals can significantly influence stability of these films. The use of an A/R coating serves to increase cell stability as well as increase J_{sc}.

The more recent study on Cu-Cr-Si cells showed that Cu does not significantly diffuse through the Cr and oxide to penetrate the Si. Cr does penetrate the oxide into the Si during prolonged use of the cell but has not seriously degraded performance. A reduced fill factor supports the need for a hermetic seal to prevent air and moisture from degrading the conductance of thin metal films and contacts. An encapsulant must be used which does not discolor or pick up dirt during extensive use in the out-of-doors.

More studies on transparent oxide heterojunction cells must be utilized to fully evaluate results on these devices. The use of various encapsulants must be studied to determine effects on long-term performance.

Acknowledgment

Dr. Brown Williams and Glenn Fowler of RCA David Sarnoff Laboratories were helpful in the Auger studies. A. H. M. Kipperman, P. Viktorovitch, G. Kamarinos, W. G. Townsend and R. L. Anderson provided data from their studies which were used in part of this paper.

STABILITY OF CONDUCTING OXIDE/Si HETEROSTRUCTURE SOLAR CELLS*

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I. INTRODUCTION

Heterojunction solar cells (HJSC's) and heteroface solar cells (HFSC's) show promise for photovoltaic energy conversion. A HJSC consists of an active semiconductor substrate and a conducting, transparent window which serves to bend the energy bands at the surface of the substrate and to act as a low resistance contact. In some cases it also acts as an anti-reflection coating. A HFSC consists of a shallow p-n junction in the active material while the window makes low resistance contact to the surface layer of the substrate. Its purpose is primarily to reduce series resistance without absorption of solar radiation, although in some cases it can also act as an anti-reflection coating.

To be practical, the characteristics of these cells must be stable for a period on the order of 20 years. In this paper we report our results on the stability of heterojunction and heteroface solar cells using Si as the active substrate and conducting oxides as window materials. The window materials used are SnO_2, In_2O_3, and a mixture of these two, commonly referred to as indium-tin-oxide (ITO). The fabrication details have been reported elsewhere.[1-3] The SnO_2 and In_2O_3 were deposited onto Si substrates by vacuum evaporation while the ITO was deposited by R. F. Sputtering.

II. EXPERIMENTAL RESULTS

A. Window Contacts

Aluminum contacts to the conducting metal oxides are initially of low resistance, but become high resistance in a matter of days. This is presumably the result of the formation of an interfacial layer of Al_2O_3 as expected from thermodynamic considerations. This can be seen from Fig. 1 where the free energy of Al_2O_3 (per unit oxygen) is shown to be appreciably lower at all temperatures than for either SnO_2 or

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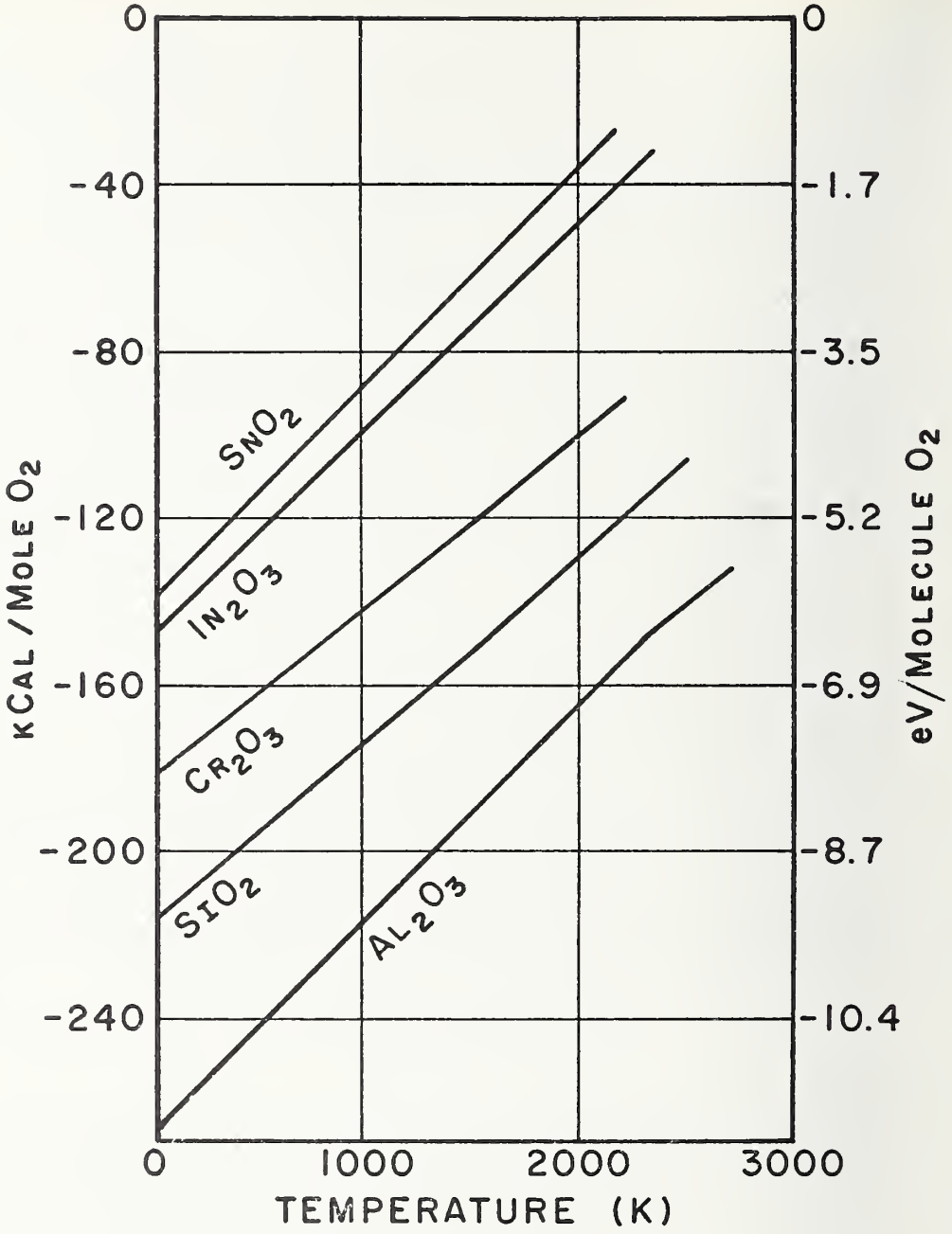
*Work supported by the National Science Foundation.


0
-40
-80
-120
-160
-200
-240
0
-1.7
-3.5
-5.2
-6.9
-8.7
-10.4
SnO2
In2O3
Cr2O3
SiO2
Al2O3
0
1000
2000
3000
TEMPERATURE (K)
KCAL / MOLE O2
eV/MOLECULE O2

In_2O_3. It is expected that the Al reduces the window material to form Al_2O_3 which is highly resistive. A barrier layer of Cr deposited before the deposition of Al prevents this degradation. Although the free energy of Cr_2O_3 is below that of either In_2O_3 or SnO_2, the lack of degradation suggests that either the reaction rate is too slow to be detected or that Cr_2O_3 is highly conductive. Mo and Ti have also been reported to act as barrier layers.[4]

B. Window/Substrate Interfaces

SnO_2/Si HJSC's

It is observed that SnO_2/n-Si cells degrade over a period of weeks at room temperature and that the degradation rate increases at elevated temperatures. This degradation is manifested primarily by an increase in series resistance. The excess resistance is localized at the SnO_2/Si interface. It is believed to result from the reaction

$$SnO_2 + Si \longrightarrow SiO_2 + Sn$$

This is consistent with the data of Fig. 1, which shows the free energy of SiO_2 well below that of SnO_2. The activation energy associated with the increase in series resistance is in the range 1.1 - 1.3 eV. Since this is the activation energy found for the diffusion of O_2^- ions through SiO_2, we believe that the degradation rate is controlled by the transport of O_2^- ions across the existing interfacial layer where they react with Si to form SiO_2. With time, the thickness of the interfacial SiO_2 layer, and thus the series resistance attributed to this layer, increases. This model predicts that the electric field established in the interfacial layer by the charge in the depletion layer of the Si tends to enhance degradation on those cells with n-Si substrates and inhibit degradation on those with p-Si substrates. This prediction is born out qualitatively as can be seen from Fig. 2, where the series resistance (normalized) is plotted as a function of time at 170° for HJSC's of SnO_2/n-Si and SnO_2/p-Si. These cells were fabricated during the same run, and except for formation of the ohmic rear contact, were subjected to the same processing steps.

As the series resistance (and thus, the thickness of the interfacial layer) increases, the I-V characteristics become increasingly sensitive to recent stress history, particularly irradiation. This is manifested by a variation of open-circuit voltage with time. It is believed that this results from optically varying the charge within the SiO_2 layer and thus the Si surface potential and the open-circuit voltage.

It is noted that the degradation of cells with polycrystalline Si substrates is appreciably more rapid than for those with monocrystalline substrates.[6] This is not understood, but it may be a result of strain at the grain boundaries.

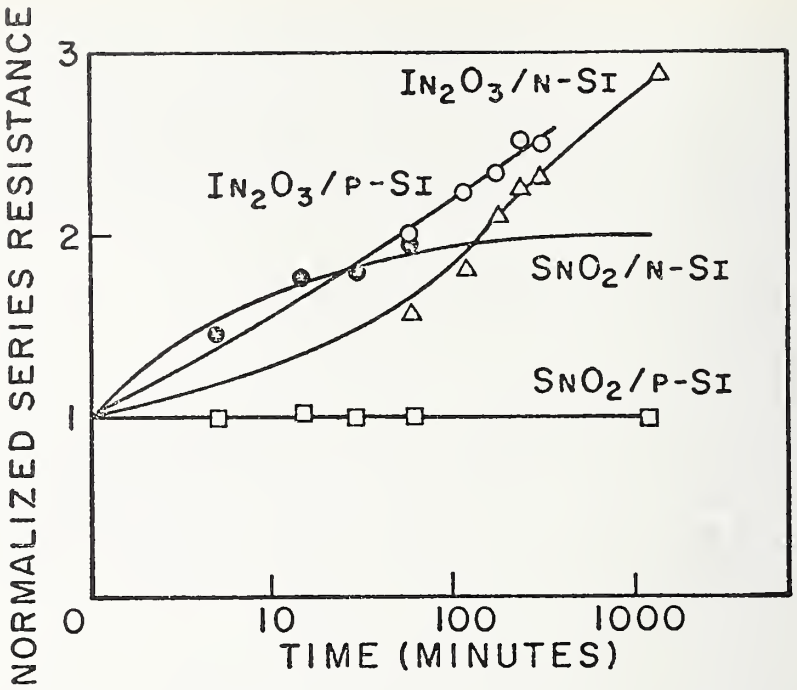


Fig. 2. Normalized series resistance as a function of time for the following heterojunctions: SnO_2/n-Si (170°C), SnO_2/p-Si (170°C), In_2O_3/n-Si (365°C), and In_2O_3/p-Si (365°C).

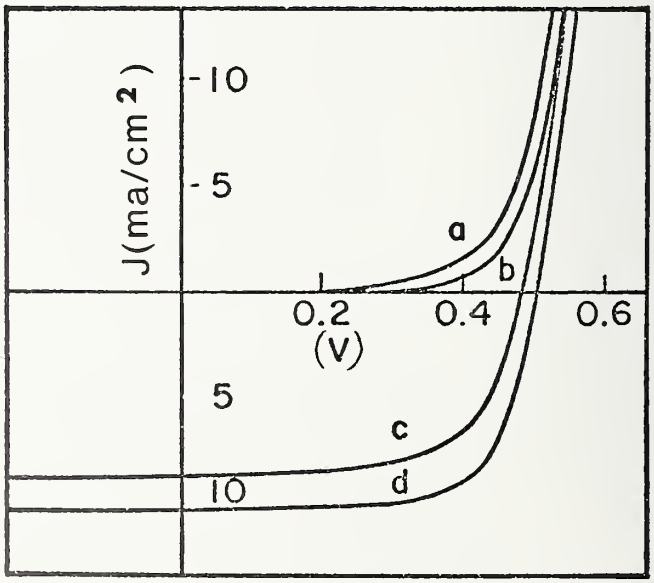


Fig. 3. Dark and AM1 J-V characteristics of ITO/p^+-n Si heteroface solar cell before (a, c) and after (b, d) annealing for 3 hours at 400°C.

In_2O_3/Si HJSC's

Degradation of In_2O_3/Si HJSC's is not observed at room temperatures although at elevated temperatures deterioration occurs much as for the SnO_2/Si cells. This can be seen from Fig. 2, where normalized series resistance is plotted as a function of time at 365°C for cells with n-Si and with p-Si substrates. These cells were from separate runs and were subjected to different processing times and so the initial states are somewhat different and the rates of increase of series resistance cannot be directly compared. Although the activation energy associated with the degradation of these cells was not measured, we assume the mechanism is the same as that for the SnO_2/Si devices. This seems plausible since the free energy of formation of In_2O_3 is only slightly less than that of SnO_2. As for SnO_2/Si devices, the In_2O_3/Si HJSC's with polycrystalline substrates degrade more rapidly than those with monocrystalline substrates.[6]

ITO/Si HJSC's

Cells made by depositing ITO of 91 mole-percent In_2O_3 and 9 mole-percent SnO_2 onto Si substrates by R. F. Sputtering showed no series resistance increase during heat treatment at temperatures up to 470°C. We conclude that either the formation of a high resistance interfacial layer does not form in this case or the growth rate is too slow to be observed under the conditions used. The In_2O_3:SnO_2 system is not well characterized, but the free energy of ITO is less than that of either constituent due to either the formation of one or more additional phases, or to the free energy of mixing.

ITO/Si HFSC's

Since SiO_2 appears not to form at the ITO/Si interface, and because degenerate (n-type) ITO is expected to form low resistance contacts with either n^+-Si and p^+-Si, Si-based heteroface cells with ITO windows appear promising. Si p^+-n and n^+-p junctions were fabricated by shallow-diffusing boron and arsenic respectively into n-Si and p-Si substrates. The ITO was then deposited by R. F. Sputtering onto the degenerate Si surface as for ITO/Si HJSC's. The cells operated as expected although the diode reverse current was appreciably larger than expected. This is attributed to the predominance of recombination current via traps introduced near the surface of the Si during the Sputtering process. These traps can be annealed out at temperatures in the range of 400-500°C with an increase in photocurrent and open-circuit voltage, and a decrease in dark saturation current and diode quality factor. This is indicated in Fig. 3 where dark and AM1 I-V characteristics of an ITO/p^+-n Si HFSC are indicated just after fabrication and after a 3-hour anneal at 400°C. After annealing, the spectral response had the same shape but was increased about 20 percent compared to that before annealing, indicating that the damage was confined to the region within about 5 um of the Si surface.

CONCLUSIONS

From thermodynamic considerations it is expected that SnO_2, In_2O_3, and ITO windows will react with Al contacts to form a high resistance layer - predominantly Al_2O_3. This is experimentally found to occur at such a rate as to increase the series resistance significantly in a matter of hours at room temperature. A layer of chrome between the conducting oxide and aluminum is effective as a diffusion barrier to isolate Al from the conducting oxide window.

SnO_2 is reduced by Si to form a high resistance SiO_2 layer at the SnO_2/Si interface and thus degrade SnO_2/Si HJSC's. The rate limiting effect is the transport of O_2^- ions across the existing SiO_2 layer where they react with the silicon substrate. The degradation is manifested by an increase in interfacial series resistance attributable to this layer, and to a fluctuation in the charge trapped in this layer. In_2O_3/Si HJSC's appear to degrade in much the same manner as do SnO_2/Si cells, although a somewhat higher temperature is required. Degradation resulting from the spontaneous formation of such an interfacial SiO_2 layer in ITO/Si cells is not observed at temperatures below 470°C. This may result from the higher dissociation energy expected from the ITO compared to that of either SnO_2 or In_2O_3. This lack of degradation permits the annealing of process-induced defects in the Si substrates.

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UNIQUE PROBLEM AREAS IN M-I-S SOLAR CELL STRUCTURES

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Introduction

The MIS solar cell configuration holds great promise for use with polycyrstalline and amorphous materials. However, unique problems can be present. To avoid these problems, extreme care must be exercised in selecting the material system to be used. We have been engaged in fabricating and testing MIS solar cell structures on both silicon and gallium arsenide. In the course of the work these unique phenomena which can occur in M-I-S structures have come to light. For convenience, we have categorized them as (1) Chemical Effects, (2) Electrical Effects, and (3) Film Structure Effects. We demonstrate these effects by presenting here material systems in which one or more occur.

(1) Chemical Effects

The electronic structure of a semiconductor surface can undergo considerable change during growth of a surface oxide or deposition of an insulator in the formation of the I-layer. These microscopic changes can manifest themselves in macroscopic behavior such as Schottky barrier height change, interface state trapping on the passing of a current, etc. Clearly the microscopic metal-semiconductor and semiconductor-insulator bonding at the surface can involve quite complex interfacial chemical reactions and localized charge redistributions.

These changes on introduction of the I-layer can be advantageous or disadvantageous[1,2] depending on the specific materials system employed. A number of MIS structures have shown increased solar cell performance with the introduction of the I-layer. An example of disadvantageous chemical effects on the introduction of the I-layer is the Pd/oxide/(n)-Si materials system. The decreased performance can be seen in Fig. 1 and 2. In Fig. 1 the diffusion potential as measured by reverse capacitance techniques for the oxide as opposed to the baseline (no intentional oxide) device indicates a lower Schottky barrier with tne I-layer present. This is also reflected in Fig. 2 which shows a larger dark current for the I-layer device. This leads, of course, to poorer photovoltaic performance for the MIS configuration than the corresponding MS device. In this particular material system there are detrimental chemical effects taking place.

We have examined the chemical nature of this system to gain insight into the interactions that can take place in an MIS system. The chemical nature of the Schottky barrier-type Pd on silicon devices was determined by complementary Auger and Ion scattering spectroscopy techniques. Post deposition analysis of metal-semiconductor (M-S) and M-I-S devices showed unambiguously that palladium silicide is formed on the M-S structure, while the presence of

an ultra-thin (< 30 Å), purposefully grown, semiconductor oxide inhibits the chemical reaction between Pd and Si in the MIS configuration.

Figure 3 shows representative ISS data obtained from (a) the Pd/Si baseline and (b) the $Pd/SiO_x/Si$ oxide structures. After removing the initial surface impurities, silicon was immediately detected in the baseline device by ISS, at t = ∿ 2 min. In the case of the oxide structures, however, Si was detected only after sputtering through the Pd overlayer (open data points). By comparing the shapes of the Si and Pd curves in the BASE vs OX-type devices, the reaction between Si and Pd is clearly indicated by ISS in the baseline structure.

A more direct evidence of silicide formation in the MS case was provided by the specturm of Auger electrons in the 40-100eV energy range. Inset A in Fig. 3 is the AES data obtained from the oxide sample after ∿ 10 min. of ion bambardment. A comparison of this spectra with that of a pure Pd standard or with handbook data[3] revealed that Pd was present in elemental form in the MIS structure.

On the other hand, a completely different AES spectra was noted from the baseline sample. An example is shown in Fig. 3, inset B, obtained after 8 min. of sputtering. Peaks characteristic of the Pd silicide formation were observed at 78, 84, 89, and 93 eV from t = ∿ 2 min. to the time at which the elemental silicon peak at 92 eV was detected.

(2) Electrical Effects

We have noticed in our work that for some systems (insulator and metal combinations), there is considerable slow trapping of charge on the passing of a current. This effect has been observed in GaAs but not on Si. Clearly these results (Figures 5, 6, and 7) suggest caution when applying some basic experimental procedures: For example, dark I-V must be taken by ramping up and down in voltage, likewise the photovoltaic response as measur by the light I-V should also be cycled. If one is unaware of these hysteresis effects in the electrical characterization of M-I-S solar cells, interpretation of cell performance in terms of fabrication procedures are difficult if not erroneous.

(3) Film Structure Effects

The nucleation and growth of some thin metal films can be a strong functic not only of the deposition rate and method of deposition, i.e. sputtering, joule evaporation, etc., but also the semiconductor surface conditions. For example, on a chemically prepared Si surface silver films of excellent quality can be easily deposited. However if the Ag is deposited on Si with ∿ 20 to 30Å of an oxide the films appears "beaded up" as observed in our TEM work (Figs. 8, 11) In such cases the porous metalization can easily provide avenues for AR materials or even ambients to enter the actual junction. Silver films with thi "beaded" nucleation have exhibited kΩ to MΩ sheet resistances. The high sheet resistance impedes the collection of photogenerated current which in turn leads to low efficiency devices.

The "beaded" nucleation on SiO_x can be overcome by using increasingly thicker metalizations ($\sim$ > 150Å as opposed to 100Å). However the increased metalization reduces the transmissivity of the incident light which in turn is seen in a reduction in the photogenerated current.

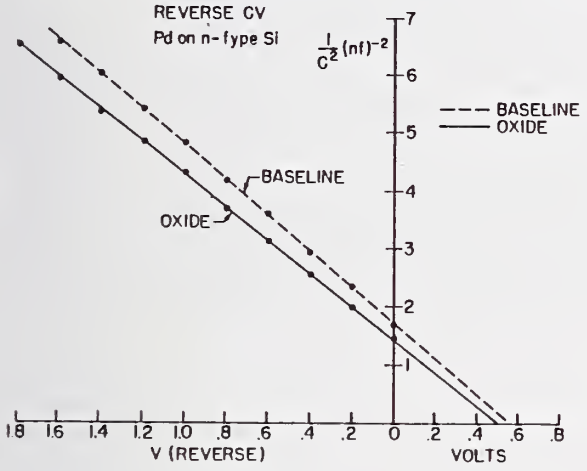

Fig. 1 Reverse bias $1/C^2$ plot for Pd Schottky barrier-type devices. The device area is 0.20 cm^2. The Pd/oxide/Si structure has a lower diffusion potential than the corresponding baseline device.

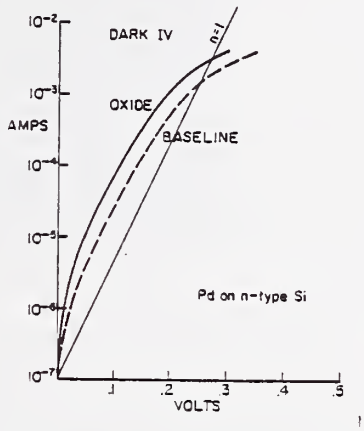

Fig. 2 Dark I-V for Pd Schottky barrier-type device. The device area is 0.20 cm^2. The effects of series resistance can be seen at the higher voltages.

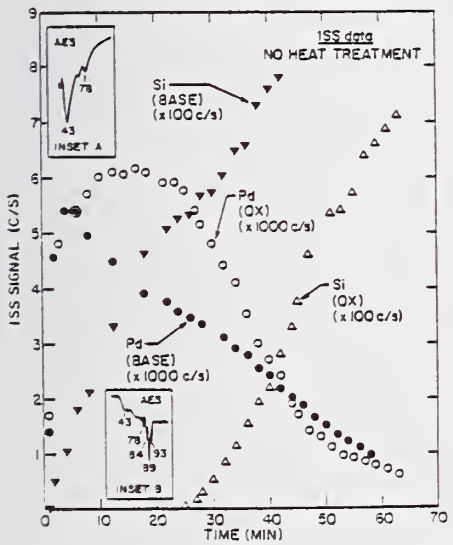

Fig. 3 ISS data obtained from (a) a Pd/SiO_x oxide (OX) Schottky barrier device (open data points), and (b) a Pd/Si baseline (BASE) type device. Inset A is the spectrum of Auger electrons obtained from the oxide sample after $\sim$10 min of ion bombardment, while inset B was obtained from the baseline device after $\sim$8 min.

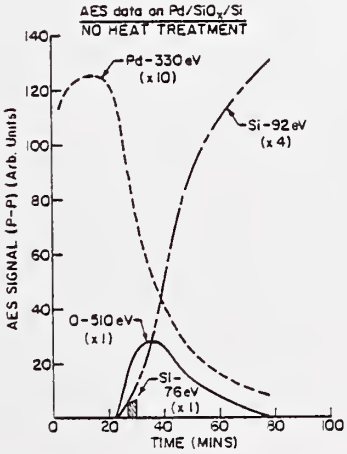

Fig. 4 AES data obtained from a $Pd/SiO_x/Si$ device as a function of ion bombardment time. The 76 eV Si (SiO_x) AES peak was detected only in the cross hatched region.

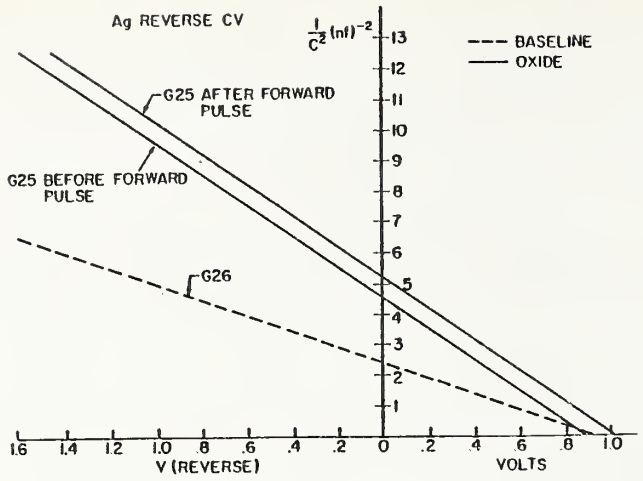

Fig. 5 Reverse bias $1/C^2$ plot for Ag Schottky barrier-type devices on GaAs. The diffusion potential is seen to shift on the oxide device after an electrical pulse. This is indicative of charge storage.

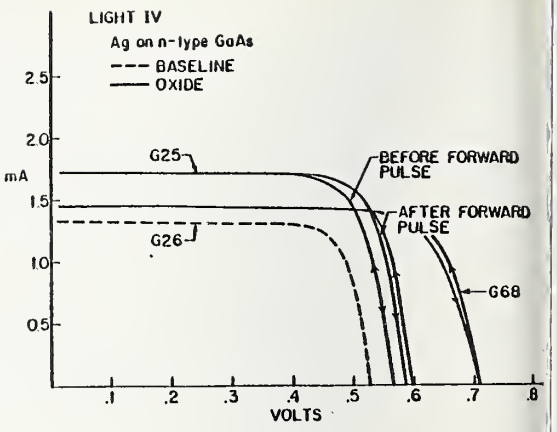

Fig. 6 Light I-V for Ag on GaAs. The shift in open circuit voltage after an electrical pulse again points to charg storage by the oxide device

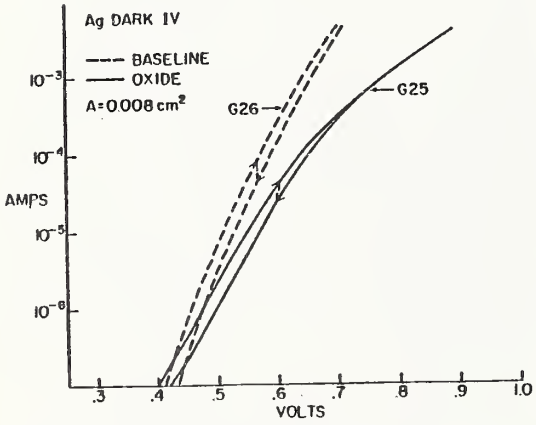

Fig. 7 Dark I-V for Ag on GaAs. The hystersis effect in the characteristic is indicative of charge storage.

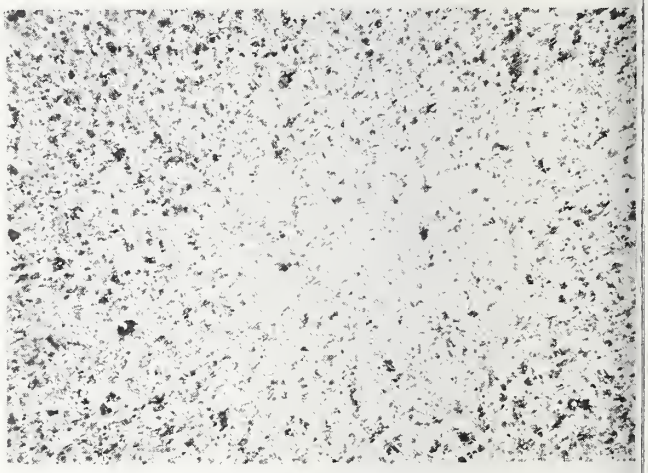

Fig. 8 TEM micrograph of a 100Å Ag film deposited on a baseline (no intentional oxide) Si substrate.

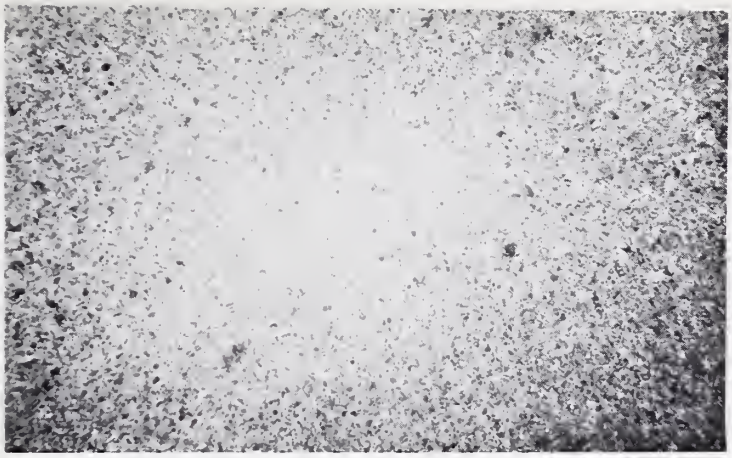

Fig. 9 TEM micrograph of a 150Å Ag film deposited on a baseline Si substrate.

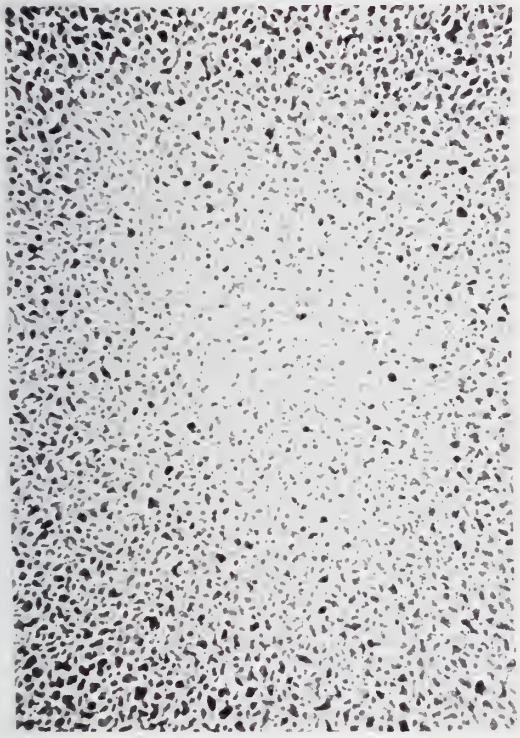

Fig. 10 TEM micrograph of a 100Å Ag film deposited on a thermally grown oxide (≤30Å). The "beading" of the metallization gives rise to a high sheet resistance.

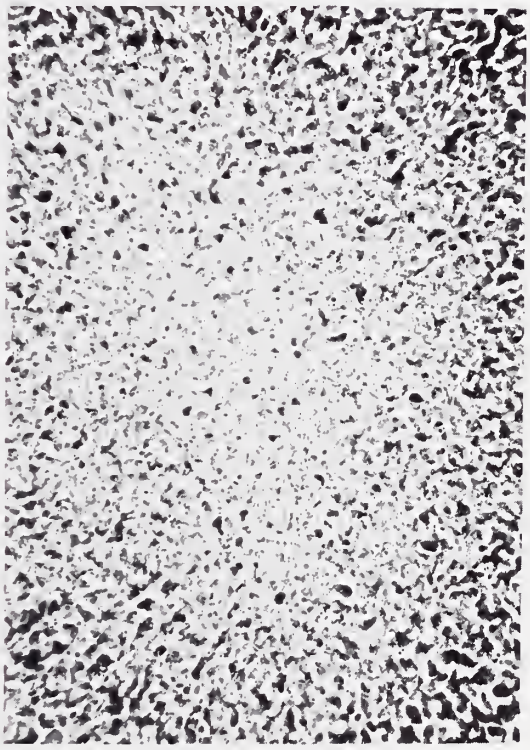

Fig. 11 TEM micrograph of a 150Å Ag film deposited on ~30Å SiO_x. The thicker metallization has reduced the sheet resistance of the film.

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1. S. J. Fonash, J. Appl. Phys. 46, 1286 (1975).

2. S. J. Fonash, J. Appl. Phys. 47, 3597 (1976).

3. E. Davis et al., Handbook of Auger Electron Spectroscopy, 2nd ed., Physical Electronics Ind., Edina, MN (1976).

RELIABILITY TESTING OF GaAs AMOS SOLAR CELLS*

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The development of gallium arsenide (GaAs) solar cells for flat plate non-concentrating arrays requires the deposition of a GaAs film no more than several micrometers thickness on a low-cost substrate. Then, because such a film is necessarily polycrystalline, a potential barrier must be introduced in a manner that will not cause serious shunting or leakage currents to flow upon illumination. One promising approach for relatively small grain GaAs films is the metal-oxide Schottky barrier. Along with the usual areas of concern for cell reliability, such as the front metallization and antireflection coating, the GaAs-substrate interface and the Schottky barrier region of the cell are areas of special concern because of the additional chemical complexity.

Figure 1 shows a cross section of one approach to polycrystalline GaAs solar cells under development at JPL with the support of the Advanced Materials R&D Branch in the Solar Technology Division of DOE.[1] The use of a recrystallized germanium (Ge) interlayer not only leads to much larger GaAs grain sizes than if the GaAs were deposited directly on a metal substrate, but also provides a low resistance ohmic contact and acts as a buffer for differences in thermal expansion coefficients between the GaAs and coated steel substrate (Fig. 2), and as a barrier to lifetime killing impurities. The Ge coefficient of expansion is nearly identical to that for GaAs; however, procedures can be taken that would be difficult with the GaAs film to assure good Ge bonding to the substrate, thereby preventing delamination. Since Ge alloys with iron at temperatures below the melting point of Ge, a passivating layer is required. This layer may be a refractory metal or alloy deposited from the vapor phase or a diffused layer of carbide or nitride compounds, for example. Such passivation techniques are now in the exploratory stage at JPL and no experience with them exists relative to reliability. It is likely that the substrate region of the polycrystalline AMOS cell will be reliable once the high temperature recrystallization and GaAs growth steps are completed successfully. The coating required for the Ge/steel interface

[1] "High-Efficiency Thin-Film GaAs Solar Cells", First Interim Report, JPL Publication 730-9, December 1977.

* This paper represents the results of one phase of research carried out at the Jet Propulsion Laboratory, California Institute of Technology, for the Department of Energy by agreement with the National Aeronautics and Space Administration.

mentioned above could be applied to both sides and edges to provide environmental stability, eliminating the need for encapsulation of the back surface.

Unlike that of the GaAs/Ge/steel region, some experience with life testing of the metal-oxide-GaAs Schottky barrier does exist. The testing being performed at JPL on single crystal versions of the GaAs AMOS solar cell shown in Fig. 1 is being done at elevated temperatures (100°C) to provide some acceleration to the life testing. Because of the fact that a number of types of barrier metal and interfacial oxide have yet to be investigated as to their potential beginning-of-life efficiency, no determination of activation energies, extrapolation of 100°C results to normal operating temperature lifetimes, nor detailed studies of the chemical dynamics, such as with Auger, ESCA, SIMS, etc., have been attempted on the particular systems discussed below.

Since the interfacial oxide layer is only of the order of 30Å thickness one would surmise that a stable metal-GaAs system without the oxide[2] is crucial to a successfully stable AMOS solar cell. Thus, testing at 100°C of unoxidized Schottky barrier solar cells with the metals Ag, Cu and Ni has been undertaken[3] (Fig. 3). The barrier heights and, hence, starting efficiencies of these metals correlate with the metal electro-negativity. From the figure, one can see that virtually no detectable changes have occurred, although Cu seems to have undergone an initial "forming" process.

However, it is well known that constituent atoms of the semiconductor can out-diffuse through gold[4] and quite likely other metals even at room temperatures. Eventually this will cause an effective barrier height reduction - possibly due to increased thermionic-field emission. A number of studies of metal-GaAs Schottky barriers have been made[5-8] showing that an interlayer of tungsten is useful for preventing degradation, such as caused

[2] The unintentionally oxidized GaAs surface nevertheless has a residual patchy native oxide (Ga_2O_3/As_2O_3) of about 18 - 20Å remaining after chemical etching and rinsing procedures prior to metallization.

[3] All cells made for life testing at 1-cm^2 fully gridded and AR-coated cells with cover glasses.

[4] A. Hiraki, K. Shuto, S. Kim, W. Kammura, and M. Iwami, Appl. Phys. Letters 31, 611 (1977).

[5] H. B. Kim, G. G. Sweeny and I. S. Heng, Inst. Phys. Conf. Ser. No. 24, Capt. 5, 387 (1975).

[6] A. K. Sinha, Appl. Phys. Letters, 26, 171 (1975).

[7] S. Guha, B. M. Arora, and V. P. Salri, Solid-State Electr., 20, 431 (1977).

[8] A. Christon and H. M. Day, J. Appl. Phys., 47, 4217 (1976).

by gallium out-diffusion, for example. However, the reduced light transmission would be unacceptable for solar cell application. In any case, it is unlikely that a diffusion barrier layer of metal can be effective for such thin films.

If the barrier metal is saturated with the element tending to out-diffuse, the metal will not behave as a sink for this process. This effect was demonstrated for the Ga/Au system,[7] where Au/GaAs barrier heights and diode ideality factors were little affected even for temperature exposures of 400°C. This approach, using flash-evaporated, Ga-saturated Au or Ag alloys, will be investigated on the JPL program.

With the addition of an oxide layer, the observed stability is reduced at 100°C - at least for the deposited oxide layer of Sb_2O_3[9] (Fig. 4). Nevertheless, the figure does show that the choice of metal can be important for reliability as well as for efficiency. Figure 5 shows that, for a given metal, Ag in this case, there are differences in oxides also. Here, a comparison is made between the unoxidized cell and cells using a native oxide grown by water vapor saturated O_2 at room temperature, a deposited (evaporated) Sb_2O_3 oxide and a deposited MoO_3 oxide. The parameter compared is the open-circuit voltage (V_{OC}), which, along with fill factor, is the photovoltaic parameter most affected by degradation. The native oxide clearly shows a less rapid degradation rate as compared to Sb_2O_3. MoO_3, on the other hand, actually shows signs of V_{OC} leveling off. It should be pointed out that these results are for one sample of each type. Also, since the deposited oxides were evaporated from a resistance-heated boat, stoichiometry control is poor. Means to flash evaporate and/or reactively evaporate oxides in an oxygen background pressure are being pursued.

Figure 6 shows the change in fill factor for the same types of oxides as in Fig. 5. Here a marked change only occurs for Sb_2O_3. The reasons for the observed degradation with time at 100°C seem to be related to the introduction of interface states within the forbidden band gap further removed in energy from the valence band edge. These states could cause a decrease in barrier height by shifting the metal Fermi level, which in turn would cause the observed decrease in V_{OC} for all oxide types investigated to date. In addition, particularly in the case of Sb_2O_3, new interface states are apparently being introduced which act as recombination centers with a large capture cross section for majority carriers (electrons). This effect would cause large increases in the reverse saturation current and diode ideality factor (n). This is observed for Sb_2O_3 as shown in Figs. 7 and 8. The decrease in n for the water vapor oxide is unexplained; however, the starting value of 1.34 for this particular sample was abnormally high.[9]

In conclusion, reliability problems with the type of GaAs thin-film structure shown in Fig. 1 are likely to occur with the enhanced barrier

[9] R. J. Stirn, Y. C. M. Yeh, E. Y. Wang, F. P. Ernest and C. J. Wu, Tech. Digest IEDM, Washington, D. C., December 1977.

height produced with AMOS processing. Life testing with several metal-oxide combinations has only recently been initiated using 100°C, laboratory air environments. Additional experiments with other deposited oxides are needed - particularly with reproducible stoichiometric oxides and with Ga-saturated metals - to identify potentially long-lived GaAs Schottky barriers.

The contributions of Dr. Y. C. M. Yeh, Mr. C. J. Wu, Mr. F. P. Ernest, and Mr. W. A. Hermann are gratefully acknowledged.

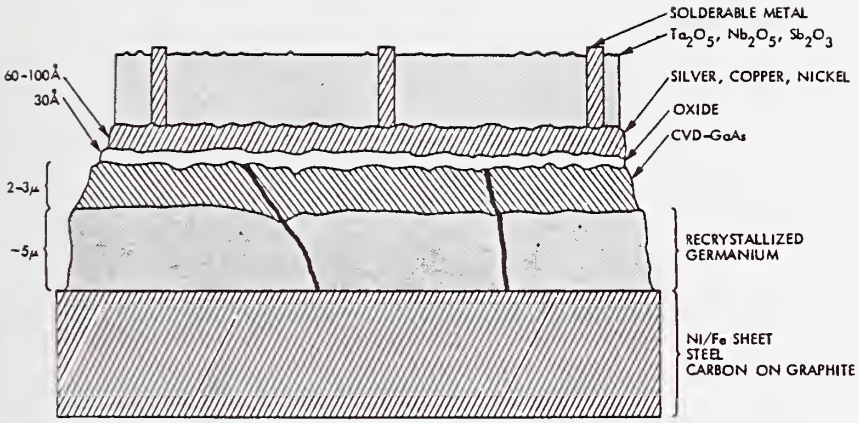

Fig. 1 Cross section of proposed thin-film GaAs solar cell.

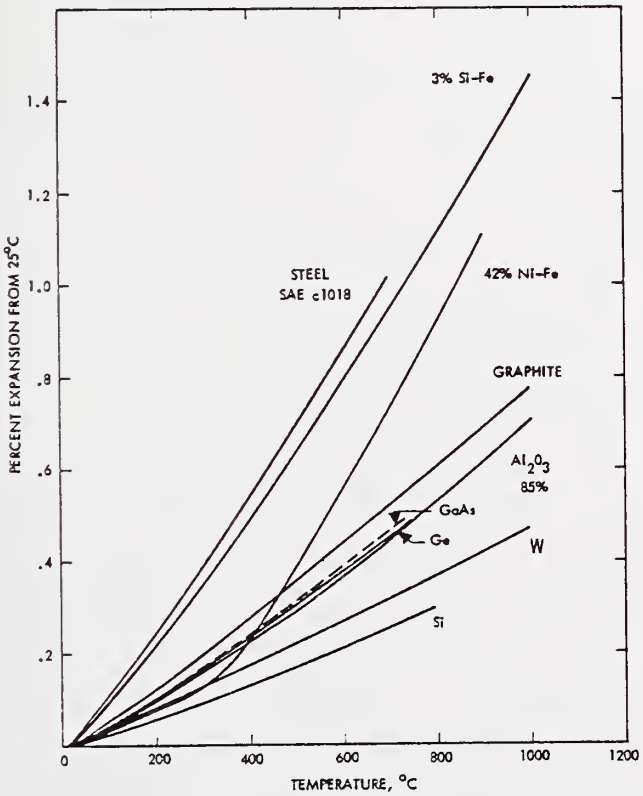

Fig. 2 Comparison of thermal expansion for some selected materials.

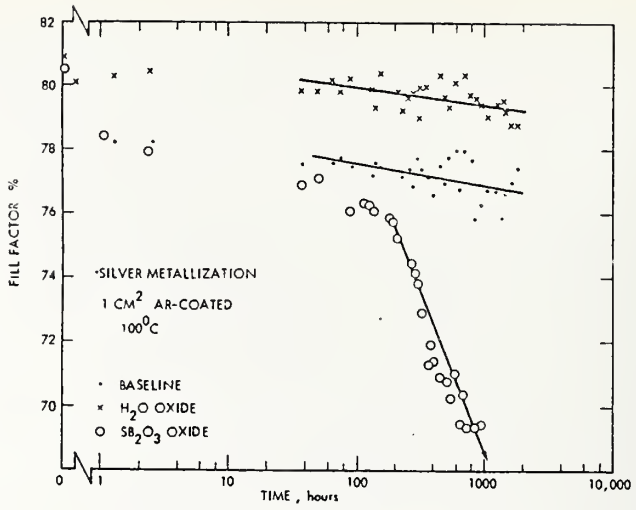

Fig. 6 Stability of fill factor with 100°C exposure in the dark.

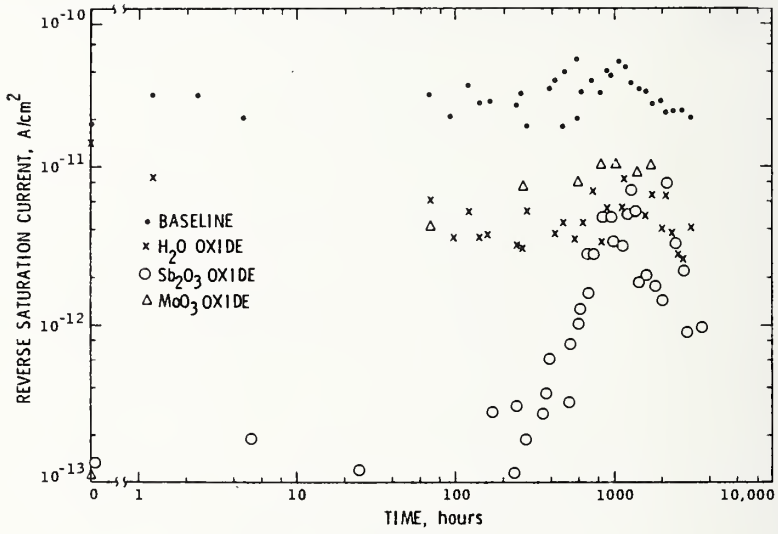

Fig. 7 Results of 100°C exposure in the dark on reverse saturation current density.

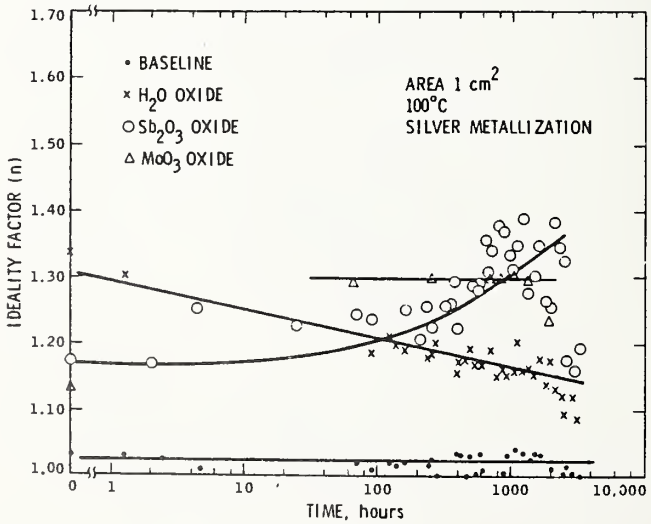

Fig. 8 Results of 100°C exposure in the dark on the diode ideality factor.

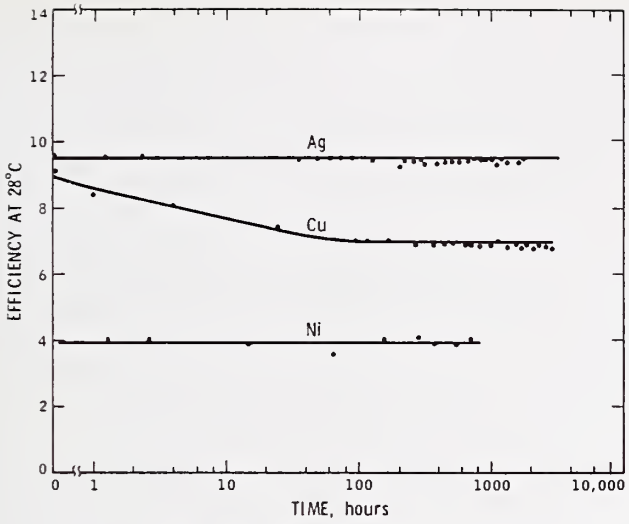

Fig. 3 Results of 100°C exposure in the dark of three SB solar cells without intentional oxidation.

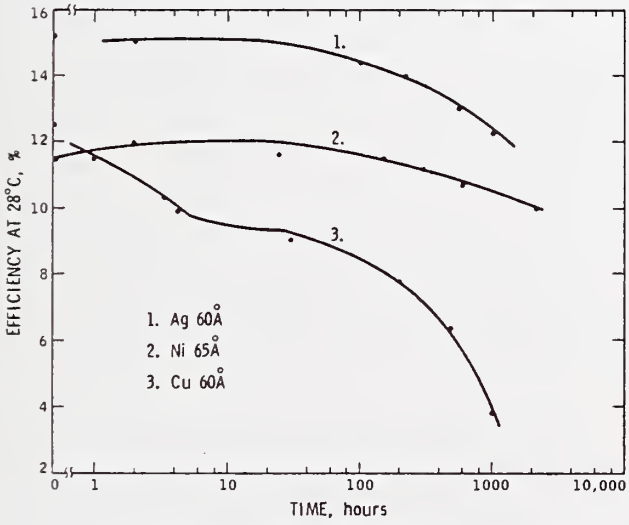

Fig. 4 Same as Figure 3, but for AMOS solar cells fabricated with 38Å thickness of deposited Sb_8O_8.

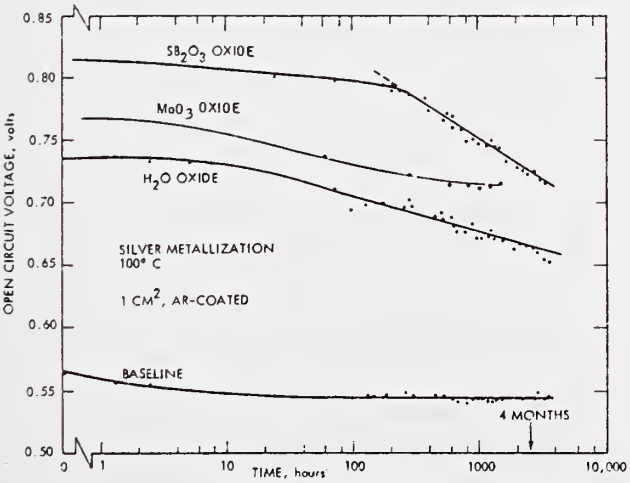

Fig. 5 Stability of V_{oc} with 100°C exposure in the dark for several types of AMOS solar cells.

STABILITY OF THIN FILM GALLIUM ARSENIDE SOLAR CELLS*

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Gallium arsenide is a promising material for thin film solar cells. Because of its sharp absorption edge and large absorption coefficient, solar radiation with energy in excess of the energy gap is essentially all absorbed within a few micrometers of the surface, and relatively short minority carrier diffusion length can be tolerated. Very little information is available regarding thin film gallium arsenide solar cells. The first cell was reported in 1967;[1] Schottky barrier solar cells of the configuration Pt/n-GaAs/Mo with Krylon or silicon monoxide as an antireflection coating was found to have most satisfactory characteristics. Under illumination at 100 mW/cm^2, the conversion efficiencies were 3%, 4.5%, and 5% for cells of 4 cm^2, 2 cm^2, and 0.2 cm^2 area, respectively. Recently, gallium arsenide films deposited on tungsten-coated graphite substrates by the reaction of gallium, hydrogen chloride, and arsine have been used for the fabrication of solar cells, and large area (9 cm^2) cells with an AM1 efficiency of higher than 6% have been prepared reproducibly.[2]

To determine the feasibility of using thin film gallium arsenide solar cells for terrestrial applications, a program has recently been initiated to investigate their characteristics as a function of temperature and their stabilities under temperature and optical stress. Some preliminary results are reported in this paper.

Gallium Arsenide Films on Tungsten/Graphite Substrates

The substrates for the deposition of gallium arsenide films were prepared by depositing a tungsten film of about 2-3 μm thickness on grade DFP or TRA graphite (POCO Graphite Incorporated, Decatur, Texas) of 1.2 mm thickness using the thermal reduction of tungsten hexafluoride at 500°C. Gallium arsenide films of 15-20 μm thickness were then deposited on tungsten/graphite substrates at 750°-775°C by the reaction of gallium, hydrogen chloride, and arsine in a gas flow system. The

*Prepared for the Division of Solar Technology, Department of Energy under Contract No. EY-76-C-03-1284.

[1]P. Vohl, D. M. Perkins, S. G. Ellis, R. R. Addiss, W. Hui, and G. Noel, IEEE Trans. Electron Devices, ED-14, 26 (1967).

[2]Shirley S. Chu, T. L. Chu, and H. T. Yang, Appl. Phys. Lett., 32, 557 (1978).

deposited films are essentially polycrystalline with weak {111} preferred orientation in some cases, as shown by X-ray diffraction examinations. The average crystallite size in gallium arsenide films is about 10 μm.

Gallium arsenide films deposited on tungsten/graphite substrates without intentional doping are all n-type with carrier concentrations in the range of 2×10^{16} to $8 \times 10^{16} cm^{-3}$ at room temperature, as determined by the differential capacitance method using silver or gold Schottky barriers. They can be doped with sulfur to yield a carrier concentration of higher than $10^{18} cm^{-3}$ by introducing hydrogen sulfide into the reactant mixture during the deposition process.

Fabrication of Solar Cells

The use of the Schottky barrier approach for thin film polycrystalline gallium arsenide solar cells is advantageous over that of the p-n junction approach; the surface recombination of photogenerated carriers is minimized and the effects of rapid dopant diffusion along grain boundaries is essentially eliminated. Although Schottky barrier cells have lower open-circuit voltage than p-n junction cells, the use of a thin oxide interlayer increases appreciably the barrier height and thus, the voltage output.[3] The MOS approach is therefore selected in this work. The use of this approach also simplifies the handling of gallium arsenide films since polycrystalline gallium arsenide oxidizes rapidly in air.

The gallium arsenide films used for solar cells were prepared by depositing successively an n^+-GaAs film (carrier concentration > $10^{18} cm^{-3}$, for reducing the gallium arsenide/substrate interface resistance) of 2-3 μm thickness and an n-GaAs film (2×10^{16} to $8 \times 10^{16} cm^{-3}$) of about 15 μm thickness on a tungsten/graphite substrate at 775°C. Immediately after the deposition process, gallium arsenide films were oxidized in situ with an argon-oxygen mixture at 100°-300°C for 0.5-2 hours, followed by room temperature treatment with oxygen saturated with water vapor for 5-10 hours. Susequent to the oxidation process, a gold film of 60-70 Å thickness was evaporated onto the surface under a pressure of less than 10^{-6} Torr, and the grid contact was formed by evaporating silver through a metal mask. A titanium dioxide film of 600-700 Å thickness deposited at 80-100°C by the hydrolysis of tetra-isopropyl titanate[4] in an argon atmosphere was used as the antireflection coating. Conducting epoxy was used to attach lead wires to the grid contact and graphite, and an iron-constantan thermocouple was also attached to the cell for temperature measurements. The cell was

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[3] R. J. Stirn and Y. C. M. Yeh, IEEE Trans. Electron Devices, ED-24, 476 (1977).

[4] A. E. Feuersanger, Proc. IEEE, 52, 1463 (1964).

then encapsulated in GE RTV 615 transparent silicone potting compound, and SS-4120 primer was used to insure a strong bond between the cell and the silicone. The AM1 efficiency of the solar cells at room temperature is usually in the range of 6 to 6.5%.

Solar Cell Characteristics Versus Temperature

Thin film polycrystalline gallium arsenide solar cells prepared in this work are 9 cm^2 in area. The current-voltage characteristics of several solar cells with silver and gold as the barrier metal were measured in the temperature range of -30°C to 80°C in the dark and under illumination with GE ELH quartz-halogen lamps calibrated with a standard silicon cell under AM1 conditions. The measurements were carried out in the order of increasing temperature; both the dark and illuminated characteristics remained unchanged after the high temperature measurements. The data on one cell with silver barrier and one cell with gold barrier are discussed here as examples.

Figures 1 and 2 show, respectively, the dark characteristics of a silver barrier cell and a gold barrier cell. The silver barrier cell appears to have a somewhat lower saturation current than the gold barrier cell in the temperature range under study. The diode parameter "n", about 2.5, appears to be similar in both cells, and is essentially independent of temperature. The high "n" value and saturation currents are presumably related to the high concentration of grain boundaries. At a given voltage, both the forward and reverse currents increase with increasing temperature as expected. The solar cell characteristics under illumination equivalent to AM1 conditions at different temperatures are given in Table 1. The open-circuit voltage decreased with increasing temperature, the short-circuit current density increased

Table 1. Solar Cell Characteristics under Illumination at Different Temperatures

	Ag barrier cell				Au barrier cell			
Temp., °C	-23.5	20	47	79	-27	21	45	79
V_{oc}, mV	800	660	570	475	680	570	520	430
I_{sc}, mA/cm^2	16.4	17.3	17.5	18.0	17.4	18.2	19.0	19.1
FF, %	58.8	55.4	54.1	49.1	58.3	59.3	58.6	55.5
AM1 Eff., %	7.73	6.34	5.42	4.20	6.90	6.15	5.77	4.56

with increasing temperature, and the conversion efficiency decreased with increasing temperature as expected. Figure 3 shows the variation of the open-circuit voltage of two silver barrier cells and two gold barrier cells as a function of temperature in the range of -30°C to

80°C. The open-circuit voltage is a linear function of temperature; the slope is -3.1 mV/°C for the silver barrier cells and that of the gold barrier cells is -2.3 mV/°C. The AM1 efficiency decreased at a rate of about 0.03%/°C for silver barrier cells and 0.02%/°C for gold barrier cells. As a comparison, the temperature coefficient of the open-circuit voltage of single crystalline $Ga_{1-x}Al_xAs$-GaAs p-p-n heterojunction solar cells is about -2 mV/°C in the temperature range of -173°-350°C, and the efficiency decreased at a rate of 0.022%/°C in the temperature range of 25° to 200°C.[5]

To determine the thermal stability of thin film gallium arsenide solar cells, the current-voltage characteristics of the encapuslated cells were first measured in the dark and under illumination at room temperature. They were then immersed in a constant temperature bath at 60°C for 24 hours, and their current-voltage characteristics remeasured. The characteristics of gold barrier cells were found to be unchanged. In the case of silver barrier cells, the open-circuit voltage and short-circuit current of the cells remained essentially the same; however, the fill factor degraded by about 9%, due to increased series resistance. It is not known if this increase in series resistance is associated with the increase in oxide thickness or the contact resistance of the lead wire. Further studies are underway.

The optical stress test was carried out by placing a gold barrier cell under high illumination conditions (approximately 325 mW/cm^2) with a 0.6 ohm load resistor. The cell was maintained at 50-55°C during the test by forced air cooling. The current through the load and the voltage across the solar cell were 378 mA and 316 mV, respectively, corresponding to a power output of 119 mW. This current and voltage remained relatively constant during a period of more than 48 hours. However, the AM1 efficiency of the solar cell at room temperature degraded by about 9% when measured shortly after the optical stress. The open-circuit voltage, short-circuit current density, fill factor, and AM1 efficiency were 530 mV, 19.6 mA, 60.0%, and 6.25%, respectively, before optical stress. The corresponding properties after optical stress were 510 mV, 19.3 mA, 57.6%, and 5.68%, respectively. Nevertheless, the characteristics of the solar cell recovered after standing at room temperature for about 4-5 hours.

Summary and Conclusions

Thin films of polycrystalline gallium arsenide have been deposited on tungsten/graphite substrates by the reaction of gallium, hydrogen chloride, and arsine in a gas flow system. MOS solar cells of 9 cm^2 area fabricated from these films with silver and gold as barrier metals have AM1 efficiencies up to 6.5% at room temperature. Their characteristics have been measured in the temperature range of -30°C to 80°C. While the temperature coefficients of open-circuit voltage and conversion efficiency of gold barrier cells are similar to those of single crystalline gallium arsenide p-n junction cells, the silver

[5] H. J. Hovel and J. M. Woodall, J. Electrochem. Soc., 120, 1246 (1973).

barrier cells have higher temperature coefficients. The gold barrier cells are also more stable than silver barrier cells after prolonged heat treatment at 60°C. Gold barrier cells have been operated under high illumination levels at 50-55°C with good stability. Although their room temperature characteristics showed some degradation after optical stress, complete recovery was observed in a few hours.

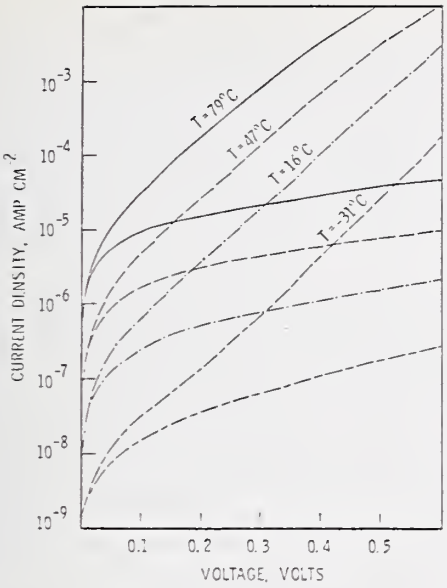

Figure 1. Dark current-voltage characteristics of a TiO_2/Ag/Oxide/n-GaAs/n^+-GaAs/W/ Graphite solar cell of 9 cm^2 area at different temperatures.

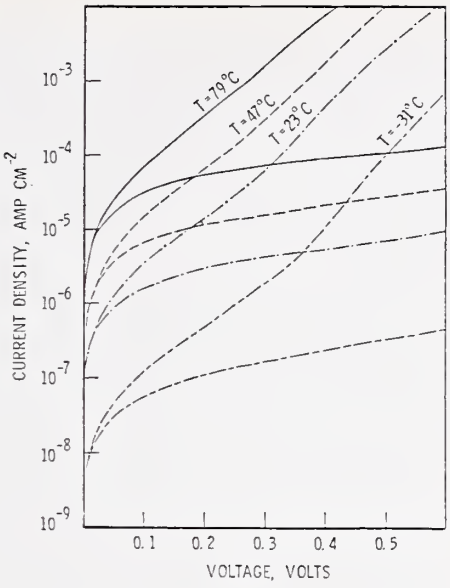

Figure 2. Dark current-voltage characteristics of a TiO_2/Au/Oxide/n-GaAs/n^+-GaAs/W/ Graphite solar cell of 9 cm^2 area at different temperatures.

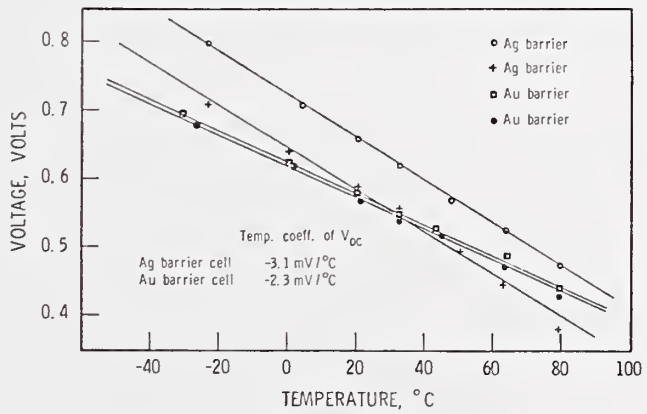

Figure 3. The open-circuit voltage of MOS gallium arsenide solar cells as a function of temperature.

STABILITY STUDIES OF AMORPHOUS SILICON SOLAR CELLS*

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Since hydrogenated amorphous silicon (a-Si:H) is a relatively new material, we have been engaged in a comprehensive program to determine the stability of a-Si:H films and devices.

One failure mode that has been recognized in a-Si:H solar cells is the evolution of hydrogen at temperatures above ~350°C. The evolution of hydrogen leaves behind dangling bonds that act as recombination centers. This interpretation is supported by data such as that shown in Figure 1 where the photoluminescence intensity decreases as hydrogen evolves from the sample (1). Other properties such as photoconductivity and short-circuit current densities (in solar cells) also decrease as hydrogen evolves from the films. Moreover, an increase is observed in the density of electron spin centers with evolving hydrogen (2).

A series of experiments were performed to measure the diffusion of deuterium in a-Si:H (3). Layered films of hydrogenated and deuterated amorphous silicon were heated for various times at temperatures ranging from 250 to 400°C, and these films were then profiled using secondary ion mass spectroscopy (SIMS). Figure 2 shows a plot of the diffusion coefficient as a function of inverse temperature. The activation energy of ~1.53 for deuterium diffusion indicates that hydrogen diffusion will not be a problem at 100°C until after more than 10^4 years.

We have also investigated the diffusion of boron and phosphorus in a-Si:H using both SIMS and Auger electron spectroscopy. Recent analyses indicate that the diffusion coefficient for phosphorus is $<3 \times 10^{-17}$ cm^2/s at 450°C, and that the diffusion coefficient for boron is $<3 \times 10^{-17}$ cm^2/s at 350°C. Thus, the diffusion of dopants is not a problem even at deposition temperatures of 300-350°C.

Another possible source of degradation is the diffusion of electrode materials into the a-Si:H. Auger electron spectroscopy has been used to show that metals such as Cr, Mo, Nb, and Ta exhibit little evidence of diffusion into a-Si:H even at temperatures of ~400°C (e.g. D_{Mo} (450°C) $\simeq 10^{-18}$ cm^2/s). However, the diffusion coefficient

*Research supported by the Department of Energy, Division of Solar Technology, under Contract No. EY-76-C-03-1286, and RCA Laboratories, Princeton, NJ 08540.

of Fe is ~3 x 10^{-15} cm^2/s at 400°C, but falls to <10^{-18} cm^2/s at 300°C. Thus, a-Si:H cells can be fabricated on Fe at 300°C but exhibit a large series resistance if fabricated near 400°C. It is likely that iron silicides are forming in the interfacial region at 400°C. Aluminum interdiffuses with a-Si:H even at 300°C, and Herd et al (4) report that Al induces crystallization of a-Si at 335°C. The presence of an oxide layer on Al inhibits interdiffusion but also gives rise to a large series resistance.

The diffusion coefficient of oxygen is ~6 x 10^{-18} cm^2/s at 450°C, but a thin naxcent oxide (~10-20 Å thick) forms on an exposed surface of a-Si:H even at room temperature. Since a-Si:H films contain considerable amounts of bonded hydrogen (~10-50 at. %), the nascent oxide is probably rich in OH groups. MIS devices utilizing the mascent oxide as a thin insulating layer exhibit degradation when exposed to air, but a heat treatment in a vacuum can reverse this degradation.

Devices made without a nascent oxide exhibit good stability, and p-i-n cells have shown no degradation after more than 2½ years on the shelf. Schottky barrier cells have been fabricated with intimate barrier contacts by etching the a-Si:H just prior to the Pt evaporation. Such cells have shown no degradation after more than one year in the short-circuit mode under continuous illumination of ~75 mW/cm^2. Moreover, these cells are relatively stable at elevated temperature. Figure 3 shows the short-circuit current density (J_{sc}) and the open-circuit voltage (V_{oc}) of a Pt Schottky barrier cell after isochronal heat treatments for 15 minutes at temperatures ranging from 100 to 400°C in air (5).

As shown in Figure 3, J_{sc} and V_{oc} were not affected by heat treatments below 200°C. V_{oc} decreases for temperatures $\gtrsim$250°C due to a decrease in the Schottky barrier height (apparently due to the formation of Pt silicides (4). Similar cells have been kept at temperatures of 150°C in air for more than 5 months without any degradation.

The recently discovered phenomenon of light-induced conductivity changes in a-Si:H does not appear to have any deleterious effect on solar cell stability (6). Prolonged exposure to light does decrease the electron lifetime measured in the dark and at low light levels, but the hole transport properties do not appear to be affected.

In summary, our studies to date indicate that a-Si:H solar cells should be stable devices under normal operating conditions.

Acknowledgments

The author thanks C.W. Magee, E.M. Botnick, and A.R. Triano for their technical assistance.

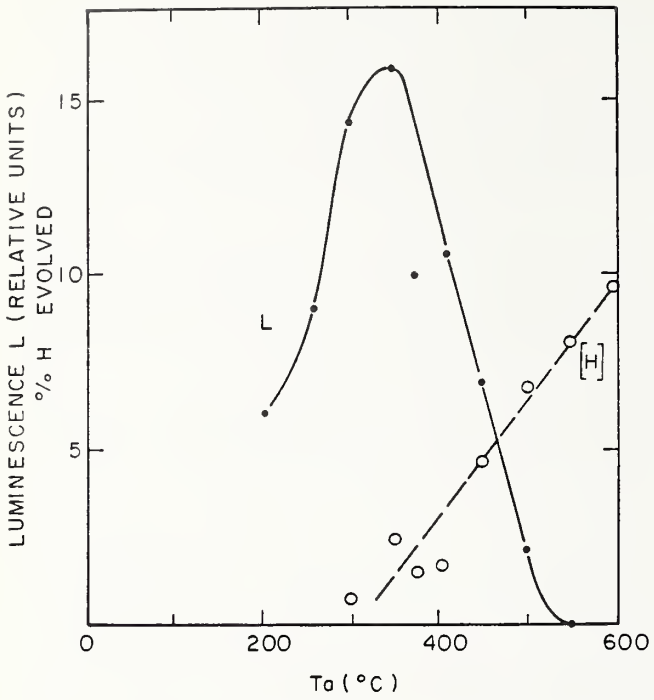

Figure 1. Luminescence intensity (L) and hydrogen evolved (H) from a-Si:H after a 30 min. anneal at indicated temperatures.

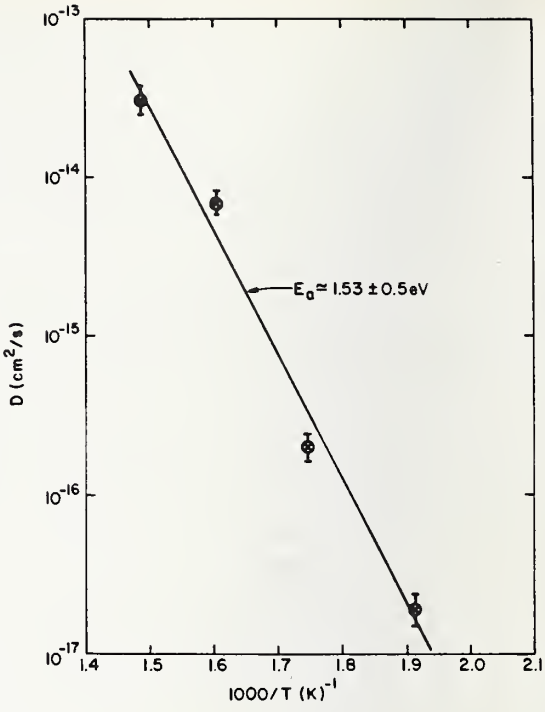

Figure 2. The deuterium diffusion coefficient as a function of 1000/T.

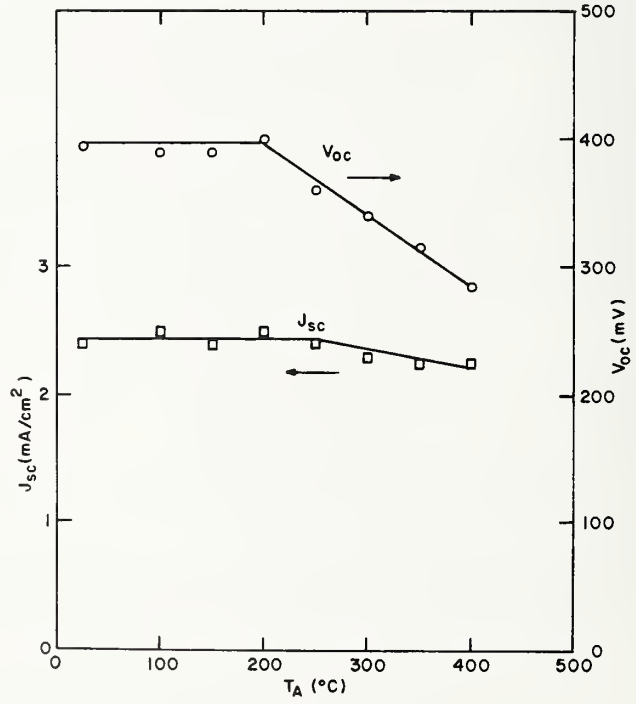

Figure 3. The short-circuit current density and the open-circuit voltage as a function of isochronal heat treatments in air. The Schottky barrier metal was ~100 Å of Pt; no antireflection coating.

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SILICON CELL SPACE PROGRAM EXPERIENCE

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ABSTRACT

This talk surveys the reasons for the high reliability of silicon solar cells made for space-uses. The possible hazards for the cells are listed, and steps taken to minimize degradation are described.

The procedures used to control cell quality are discussed, along with brief recounting of some problems encountered.

Finally the implications of the space-cell experience for thin film cells are given, along with some predictable instability areas for thin film cells.

INTRODUCTION

For over twenty years silicon solar cells have performed with high reliabilit on many space missions. They have operated for long periods and have not caused any mission failures. These cells must have high output (to reduce area requirements), minimum weight, good radiation resistance, and stability for a long operational life to work off the high costs of launching.

This paper does not reveal any secrets which can help the present audience, to ensure the stability of thin-film cells. The space-cell reliability is the result of enforcing very tight specifications, by close control of all process steps, by careful in-line monitoring, as well as by stringent acceptance tests.

The additional personnel and paperwork required to provide this control add considerable cost to the cells. Clearly thin film cells which must have very low costs cannot afford to use such an expensive system.

Despite this, we will see that space-cell experience has given some guideline which can help in these workshop activities, particularly since much of the effort spent on space-cell process control is needed to protect cell arrays against as much as six months of relatively mild exposure to the terrestrial environment.

POSSIBLE HAZARDS TO SPACE CELLS

Table 1 lists the main hazards which space-cells must survive successfully. Tests to ensure pre-orbit survival comprise about half of the total effort.

TESTS TO ENSURE STABILITY

Table 2 shows how the chance of degradation is reduced by means of a series of tests. These tests include in-process tests, acceptance sampling tests and finally qualification tests. The in-line tests include many mechanical tests, and verification tests to show that the main cell process steps (diffusion, contacts and AR coating) have been performed satisfactorily. The acceptance tests are usually carried out on statistically significant samples: testing does not always provide the same conditions which space-cells many encounter in operation.

These tests are determined using a rigid set of procedures, developed cooperatively by the array fabricator (usually the prime contractor) and the cell manufacturer. This cooperation is described in Table 3, (A, B, C), where other precautions are also shown. The specification of a narrow range of good I-V properties (select the best cells only), can be used to advantage in process control; this is because meaningful conclusions can be drawn on the cell properties (series or shunt resistance) or on silicon properties (diffusion length) using the cell I-V characteristics which are sensitive to change; I-V data can also be used to monitor the results of environmental tests.

NOTE: At this stage in the talk, typical examples of detailed cell properties and specifications, lot traveler forms, and process specifications were shown rapidly to indicate the complex paperwork involved.

It is clear from this section that for very low cost cells, a similar detailed test sequence would not be workable.

Next we will discuss some of the main space-cell problems which have arisen and have been solved, because they can indicate possible problem areas for thin film cells.

SOME SPACE-CELL PROBLEMS

Table 4 lists some space-cell problems. In some cases these problems were solved soon after their recognition, during the same production run. In other cases, additional development of improved cell processes was needed to increase stability.

Early solar cells used electroless plating plus soldering to form contacts. Adhesion problems with electroless plating were difficult to solve by use of sintering, because of interaction between the plating materials and the shallow diffused layers needed for good cell output. These adhesion problems were reduced with advent of polished silicon wafers with the titanium-silver contact system. This system had moisture-sensitivity under accelerated humidity-temperature testing; a solution was available, either by solder coating the silicon, or preferably by adding palladium to the metal system, to reduce corrosion of titanium by water. Occasional delamination problems of contacts or coatings were solved by attention to the cleaning procedures used. In some cases, adjustment of the deposition conditions, or use of different heat treatments (or atmospheres) improved adhesion.

Solder coating has some advantages in reduced moisture resistivity and ease of interconnection. However, there are disadvantages caused by the normal temperature cycling experienced by satellites; some improvement in temperature cycling capability can be provided by addition of processes to provide controlled thinner solder thickness.

Much work on cell designs resulted in additional radiation protection; the solutions involve change of configuration to use P-type base silicon, use of covers, use of higher resistivities and general control of purity levels of the materials, especially of the silicon. This set of problems are not foreseen for any large scale terrestrial use (except in the case where large orbiting satellites are used as power stations).

UV and photon problems have not been serious for space-cells. However, care is needed for thin film cells, because they should be designed for long operating lines ($\sim$20 years) and may include less pure materials or structures which could become unstable under prolonged exposure.

IMPLICATIONS FOR THIN FILM CELLS

Finally we indicate, in Table 5, some possible implications for stability of thin film cells which are suggested by examination of the space cell experien

We have emphasized that the high cost monitoring and control system used for space-cells cannot be tolerated within the constraints for low cost operation We can predict some possible problem areas for thin film cells. We believe that for all cells the contacts will pose a major problem, both in filling a wide range of necessary requirements (cost, good conductivity, etc.) and in reducing the chance of corrosion or of failure under temperature cycling. In some cases (e.g. amorphous silicon), the contacts comprise the bulk of the cell.

In order to provide effective low cost operation with minimum energy payback periods, the cells must operate for long periods.

Experience has shown that when thin films are used, there are increased chances of interlayer movement, usually with adverse effects on cell properti Also it is reasonable to assume that low cost cells must display a wider rang of I-V properties.

Automated production will probably be required to give low cost cells; as usual, automation must be applied to a well proven basic process sequence.

Present thin film cells present a very wide range of possible materials and processes, (as shown by the varied subjects covered in this workshop) and thi makes stability tests more difficult.

Some general quidelines can be carried over from the space work. These quide lines involve cooperation between cell makers and cell users, the choice of realistic tests, effective encapsulation to reduce interaction with the atmoshphere, and a continual search for metallurgically stable systems.

CONCLUSION

The main message is that mostly the methods used to ensure stable space-cells are ruled out by costs, even when these methods involve stability before cells are launched. Also thin film cells may have special problems (exemplified by Cu in CdS, or H_2 in amorphous silicon), but will also share general problems (UV exposure, temperature cycling, and corrosion effects). Some preliminary areas of concern have been signalled by the space-cell experiences.

A good balance must be maintained between continuing innovations, and the inclusion of realistic tests to indicate how thin film cells will operate. There is no question that the whole field of thin film cells will provide a fruitful field for materials scientists, and process quality control, to ensure stability and maximum operating effectiveness on a large scale, within very severe cost limitations.

TABLE 1

POSSIBLE HAZARDS TO SPACE CELLS

THROUGH LAUNCHING

MECHANICAL BREAKAGE

CORROSION (CONTACTS)

IN-ORBIT

THERMAL CYCLING

UV DEGRADATION (COVERS)

RADIATION DEGRADATION

PLASMA BUILDUP

MODERATE TEMPERATURES FOR LONG TIMES

NOTE: MANY OF THE SPECIFICATIONS ARE INTENDED TO REDUCE LOSSES BEFORE CELLS ARE IN ORBIT.

TABLE 2

HOW DEGRADATION IS MINIMIZED

QUALIFICATION TEST

GENERALLY SAME AS THE ACCEPTANCE TESTS BUT AT A TIGHTER AQL (ACCEPTANCE QUALITY LEVEL) OR LTPD (LOT TOLERANCE PERCENTAGE DEFECTIVE).

IN-LINE TESTS

MECHANICAL	DIMENSIONAL CONTROL MECHANICAL DEFECTS WEEDED-OUT GOOD QUALITY SILICON CAREFUL CUTTING, POLISHING CAREFUL HANDLING
CONTACTS & COATING	CLOSE MONITORING CLEAN DEPOSITION PURE (EXPENSIVE) MATERIALS SOLDER (RESTRICTED) OR PALLADIUM TO REDUCE CORROSION

ACCEPTANCE SAMPLING TESTS

HUMIDITY TEST (PLUS PULL TEST)
CONTACT PULL TEST (OR TAPE TEST)
BONDABILITY
VIBRATION, ETC. (ARRAYS)
UV. RADIATION TESTS
TEMPERATURE SHOCK
TEMPERATURE CYCLING
BOILING WATER (ERASER)

TABLE 3

HOW IS QUALITY MAINTAINED?

A. PRIME CONTRACTOR

PREPARES DETAILED CELL SPECIFICATION (REFLECTS MISSION NEEDS) AND SUPPLIES RESIDENT "SOURCE INSPECTOR".

B. CELL MANUFACTURER

SUPPLIES CELL PROCESS SEQUENCE WHICH CONTAINS MUCH IN-LINE PROCESS, Q.A. CONTROL (ESPECIALLY VISUAL REJECTS) AND CONFIGURATION CONTROL (WHICH MEANS NO CHANGE IN PROCESS OR MATERIAL WITHOUT PRIOR APPROVAL FROM PRIME CONTRACTOR).

C. FEEDBACK LOOP

MAINTAINED BETWEEN ARRAY FABRICATOR AND CELL MANUFACTURER (ENGINEERING, Q.A. GROUPS). CELLS CONSTANTLY ASSESSED FOR ACTUAL END-USE. ARRAYS WELL DESIGNED (STRESS RELIEVED INTER-CONNECTS, ADHESIVE CONTROL).

D. OVER SPECIFICATION (REDUNDANCY)

E. "CUSTOM-BUILT" CELLS

F. NARROW RANGE OF GOOD I-V PROPERTIES

TABLE 4

SOME SPACE-CELL PROBLEMS

NOTE: MOSTLY WERE REMEDIED DURING THE PRODUCTION RUNS.

EXAMPLES

ELECTROLESS NICKEL PLATING (ADHESION)

P+/N → N+/P (RADIATION)

TITANIUM-SILVER (MOISTURE)

CONTACT OR COATING (DELAMINATION)

SOLDER THICKNESS (THERMAL CYCLE)

SHADOW EFFECTS (ARCING)

NUCLEAR TESTS (RADIATION DEGRADATION)

PHOTON DEGRADATION

TABLE 5

IMPLICATIONS FOR THIN FILM CELLS

SPACE CELL RELIABILITY AIDED BY HIGH COSTS, AND BY HIGH QUALITY SILICON. MOST PROBLEMS IN CONTACTS, AND INTERFACE CONTROL.

THIN FILM CELLS MAY HAVE:

(i) CONTACT PROBLEMS.

(ii) NEED FOR LONG-LIFE STABILITY.

(iii) ENHANCED INTERLAYER MOVEMENT (THIN LAYERS, LESS PERFECT STRUCTURALLY).

(iv) MINIMUM MONITORING AND CORRECTIVE ACTION BECAUSE OF LOW COSTS.

(v) LESS CONTROLLED I-V PROPERTIES.

(vi) MANY OPTIONS TO CONSIDER IN MATERIAL AND PROCESS COMBINATIONS.

(vii) AUTOMATED PRODUCTION (NEED WELL-PROVEN PROCESS).

HOWEVER, DEVELOPMENT SHOULD INCLUDE:

(a) CLOSE INTERACTION (CELL MAKERS; ARRAY AND SYSTEMS GROUPS).

(b) STRESS AGING TESTS, AS WELL AS REAL-LIFE TESTING.

(c) EFFECTIVE ENCAPSULATION.

(d) SEARCH FOR METALLURGICALLY STABLE SYSTEMS.

RELIABILITY CONCERNS AND LIFE TEST PROCEDURES FOR CONCENTRATOR SOLAR CELLS*

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As concentrator solar cell technology prepares to enter the commercial market, a more complete knowledge of the expected operating life and the basic degradation mechanisms limiting long term performance becomes a necessity. Although only limited life-test data on concentrator solar cells is presently available, most degradation mechanisms are predictable though not well understood. In this presentation the factors which would be expected to be of concern in solar cell reliability are outlined, and several types of life test procedures[1] are described. Some preliminary results of recent life testing on Si and AlGaAs/GaAs concentrator solar cells are also discussed.

The reliability of concentrator solar cells must be considered in relation to the reliability of the concentrator system as a whole. This includes the concentrator optics, the tracking system, and thermal heat sinking and electrical contacting of the solar cell array. Although such problems are often of a less fundamental nature than the internal physical limitations of the individual cells, they may still represent substantial technological difficulties. However, in this discussion the more basic problems relating to single cell reliability will be stressed.

Because of the rigorous environmental conditions in which concentrator solar cells must operate, a large number of possible causes of degradation arise. Among the conditions and problems which must be considered are the following:

1) Temperature
2) Thermal cycling
3) Mechanical stresses
4) Current density
5) Impurity and defect diffusion
6) Non-uniform illumination
7) Current and voltage transients
8) Corrosion by moisture and atmospheric contaminants
9) Ultraviolet radiation

*This work was supported by the United States Department of Energy (DOE) under contract number AT(29-1)789.

†A United States Department of Energy Facility.

The effect of temperature is likely to be one of the most important reliability concerns in concentrator solar cells since so many material parameters are temperature dependent and higher cell operating temperatures will usually be involved. Factors such as the intrinsic carrier concentration, lifetime, and mobility are all functions of temperature. The effect of thermal gradients across the cell must be considered. Degradation resulting from the diffusion of impurities and defects is also a temperature dependent process. Although the diffusion coefficients of most impurities are extremely small at the expected operating temperatures of 30-100°C for Si cells and 40-200°C for AlGaAs/GaAs cells, diffusion may become significant if the desired operating life is 20 years or more.

The diurnal temperature cycling which a solar cell experiences in operation also presents a problem if mismatches are present in the thermal expansion coefficients between the cell and its mounting and contacting. The resulting mechanical stresses could cause cracking of the cell or the contacts, or a loss in thermal heat sinking.

The high current densities typical of concentrator cells can also contribute to a deterioration in device performance. High current and electric field levels may accelerate degradation mechanisms such as electromigration, defect formation, and recombination-enhanced defect migration.[2] The diffusion of impurities and defects has been suggested as being a major factor in the degradation of GaP light-emitting diodes[3] and AlGaAs/GaAs double-heterostructure lasers.[4]

Due to the significant series resistance in present day solar cells, non-uniform illumination can degrade the conversion efficiency of the cells, although this effect can be reduced by proper cell design.[5] The current and voltage transients caused by temporary shadowing by clouds or a solid object can also be of considerable concern. In solar cell arrays, a common practice is to shunt series connected cells in the array with diodes to protect each cell from high reverse bias conditions.

Corrosion is also a major problem with concentrator solar cells, since the elevated temperatures involved would be expected to facilitate the corrosion. Corrosion can be caused by moisture or chemical attack by various atmospheric contaminants such as sulfur oxides. To protect against those problems, encapsulating layers such as Si_3N_4, various glasses, and organic materials are being investigated. Pinholes in this encapsulating layer can result in eventual failure of the device since contaminants can then seep beneath the encapsulant and cause it to blister and peel. Other environmental effects which must also be addressed are abrasion by dust and hail. Such abrasion problems are, of course, most directly related to the concentrator array and optical system as a whole, and are not fundamental cell problems.

Ultraviolet radiation has been known for some time to cause degradation of certain plastics, adhesives, and other organic materials. This possible mode of degradation in Fresnel lenses and encapsulants must therefore be considered. However, this effect is expected to be

relatively minor for acrylics. A life test[6] of acrylic plastic has indicated only a 10% decrease in the total integrated transmittance of the solar spectrum after 21 years of outdoor weathering. Most of the decrease was apparently due to dust abrasion, since a polished specimen of aged material showed only a 3% decrease in transmission across the solar spectrum.

In order to characterize the performance and durability of a photovoltaic array in a reasonable length of time it is necessary to subject the array to various accelerated aging tests.[7] Since concentrator technology is still very new it is especially desirable that such aging information be obtained as quickly as possible so that design flaws may be corrected, and alternative fabrication processes and materials be selected. Although many types and combinations of accelerated aging tests are possible, the following three tests are the most basic and therefore should be given highest priority.

1) Constant temperature aging
2) Temperature-humidity cycling
3) Combined temperature-illumination aging

The above tests are primarily meant as tests of individual solar cells and their mounting and contacting, and modules with their associated optics. In concentrator applications there are additional system tests which are also necessary. These include the degradation of any plastics and adhesives from ultraviolet light, the effect of wind and loading stresses on the array mounting and tracking system, and the resistance of the cell coverings and the optical components to dust abrasion and hail impact.

The purpose of constant temperature aging is to determine if there are thermally activated degradation mechanisms in the cell. Since these processes would be quite slow at normal operating temperatures, elevated temperatures of 300°C or higher may be necessary to make them apparent. The results could then be extrapolated to give an estimate of the effective life at lower temperatures. In cases where substantial degradation was taking place, one would want to supplement this data with various analytical techniques such as secondary ion mass spectrometry, transmission electron microscopy, and transient capacitance spectroscopy. Correlation between these methods would be helpful in identifying the degradation mechanism if the diffusion of impurities or defect formation and migration was involved. To insure the test was only determining temperature related effects, it should be first performed in an inert atmosphere of Ar or dry N_2. This avoids extraneous problems related to the encapsulant and atmospheric contaminants. It would, of course, be informative to perform this test a second time in ambient air with 100% relative humidity. It is known that the indiffusion of oxygen or water vapor causes degradation in some materials. A notable example is oxide formation in AlGaAs with a high Al content.

The second type of life test, temperature-humidity cycling, is designed to test for various corrosion effects and the influence of

diurnal freeze-thaw cycling. Penetration by moisture and other contaminants can be investigated in such testing, although the rate of corrosion is not necessarily accelerated. A typical two hour test cycle, all performed in an environment of 100% relative humidity, could be as follows: heating the cell slowly to 200°C in 15 min, holding at that temperature for 30 min, cooling the cell slowly to -20°C in 30 min, holding at that temperature for 30 min, and finally heating the cell back to room temperature in 15 min. Such a cycle could be repeated 12 times a day. In addition, temperature-shock cycling, where the cell temperature is rapidly changed from -20°C to 250°C in 5 min or less, can be used to investigate the effect of thermal expansion stress on the cell and its mounting and contacting.

The third type of test, combined temperature-illumination aging, is one in which the cell is operating during the test. It is designed to measure the degradation under both high temperatures and high solar concentrations. The test parameters could be 100°C and 200 suns for Si solar cells, and 300°C and 1500 suns for AlGaAs/GaAs cells. Comparison of this test data with the results of constant temperature aging would give information regarding the degradation directly due to high light intensity and current levels.

In evaluating the performance of a solar cell there are several important device parameters which must be monitored. The most basic device parameters include the cell series resistance, the shunt resistance, the diode factor, and the reverse saturation or dark current. These are determined from the current-voltage (I-V) characteristic of the device. The minority carrier diffusion length is also an important device parameter. The short circuit current, the open circuit voltage, and the fill factor (a measure of the sharpness of the "knee" of the I-V curve) are affected by all these parameters.

At this time only very preliminary life test data is available for either Si or AlGaAs/GaAs solar cells. No extensive tests have been performed, and knowledge of expected operating lives and potential degradation mechanisms is minimal. In the following discussion the data is presented primarily for its tutorial value in pointing out the kind of information which can be derived from such tests, and is not meant to represent conclusive findings.

In AlGaAs/GaAs devices a major problem has been with pinholes in the Si_3N_4 antireflection coating. Consequently, the first constant temperature aging experiments utilized an atmosphere of H_2. The results of this work, performed by James et al.[8] at Varian, are shown in Fig. 1. In this figure the open circuit voltage (V_{oc}) as a function of time is shown for cells held at four different temperatures ranging from 280 to 425°C. The cells were not illuminated while being held at the high temperatures. The V_{oc} data was taken at an illumination of approximately 4 suns. The open circuit voltage is observed to decrease substantially for temperatures of 346 and 425°C. However, no significant change is seen for cell temperatures of 280 and 325°C after 300 hours.

If the time shown in Fig. 1 for V_{oc} to decrease to 80% of its initial value is plotted versus reciprocal temperature on a semilog graph, the straight line shown in Fig. 2 results. From the slope of this line, an estimate of the activation energy is derived. The data in Fig. 2 represents an activation energy of 1.7 eV, characteristic of the diffusion of some impurities in GaAs. This information would be useful in determining the degradation mechanism by comparing it to elemental diffusion distributions obtained from a profiling technique such as secondary ion mass spectrometry. It is interesting to note that if the data in Figs. 1 and 2 are representative, the operating lifetime at 200°C is projected to be several hundred years.

Operation of Si cells[9] which utilized an Al/Ag front contact grid revealed that corrosion of the contact occurs within several months of exposure to air. Presently a Ti/Pd/Ag metallization is employed and has been found to be a more stable system. The Pd acts as a corrosion inhibitor.

In a temperature-humidity test, several Si cells with the Ti/Pd/Ag front metallization have been aged in the dark in 100% relative humidity at temperatures of 40 and 90°C. Presently still in progress, this test has revealed no significant changes in the electrical properties of the cells or in the adhesion of the front and back contacts after seven months.

One Si cell has been aged at 400°C in an Ar atmosphere for 53 hours to investigate temperature related degradation. A sample without the Si_3N_4 coating was used because it was desired to observe the electrical characteristics before the effective anneal of 30 min at 280°C during the Si_3N_4 deposition. The results are therefore not representative of a finished device, but are included in the present discussion as an informative example about what can be learned about degradation from the cell's I-V curve. Testing on baseline production cells is currently in progress.

In this test no significant changes were seen in the open circuit voltage or in the series resistance at one sun illumination. However, the short circuit current (I_{sc}) increased by 20% in 53 hours, and the fill factor decreased from 0.82 to 0.61. The increase in I_{sc} is believed to be due in part to the formation of a thin surface SiO_2 layer, which is known to decrease the front surface recombination velocity. The reason for the decrease in fill factor can be seen by plotting the I-V curve of the device at different times during the test. In Fig. 3, log $I + I_{sc}$ is plotted versus V to give a shifted I-V curve so the diode equation can be used to determine I_o, the reverse saturation current, and n, the diode factor. Initially the I-V curve corresponds to that of a diode with n = 1.15 and reverse saturation current density $J_o \sim 10^{-11}$ A/cm^2 for voltages greater than ~ 0.45 V. The maximum power point voltage is ~ 0.5 V in this case. After 53 hours at 400°C, the I-V curve corresponds to a diode with $n \sim 8$ and $J_o \sim 10^{-4}$ A/cm^2 for voltages less than ~ 0.54 V, and to a diode with the initial n and J_o

values for larger voltages. The increase in J_o and n indicates additional recombination and other leakage currents are present. Changes in the I-V curve in the region of the maximum power point are therefore responsible for the observed decrease in fill factor. It should be noted, however, that aging at 400°C is a rather severe life test.

Although the possible modes of degradation in concentrator solar cells are many, until extensive life testing experiments are completed, we will not know the true extent of the problems to be faced. Though only preliminary, the present results are encouraging.

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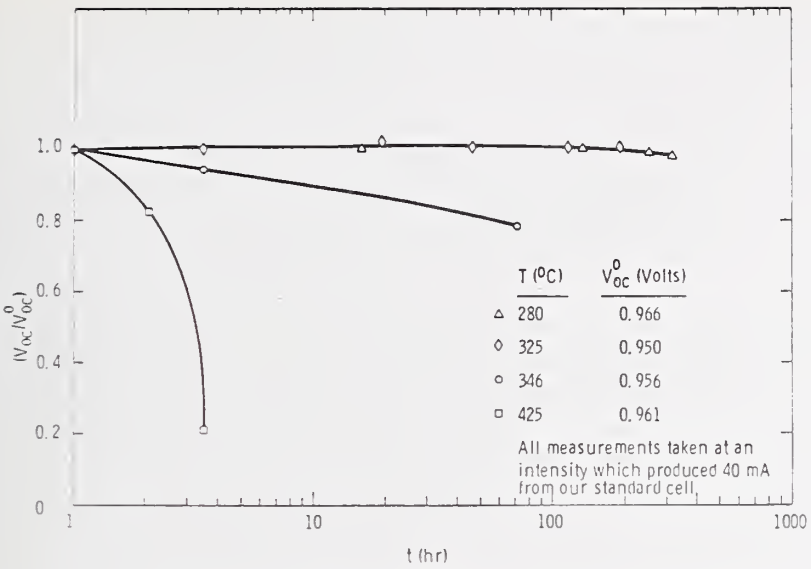
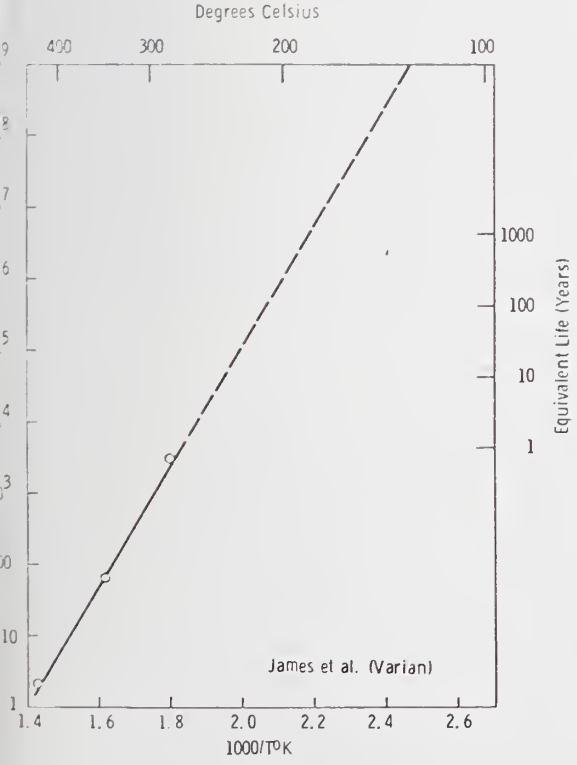


Fig. 1 Open circuit voltage versus time for four cells held at different temperatures in H_2. The V_{oc} measurements were taken at room temperature.



g. 2 Arrhenius plot of the time shown in Fig. 1 for V_{oc} to decrease to 80% of its initial value versus reciprocal temperature.

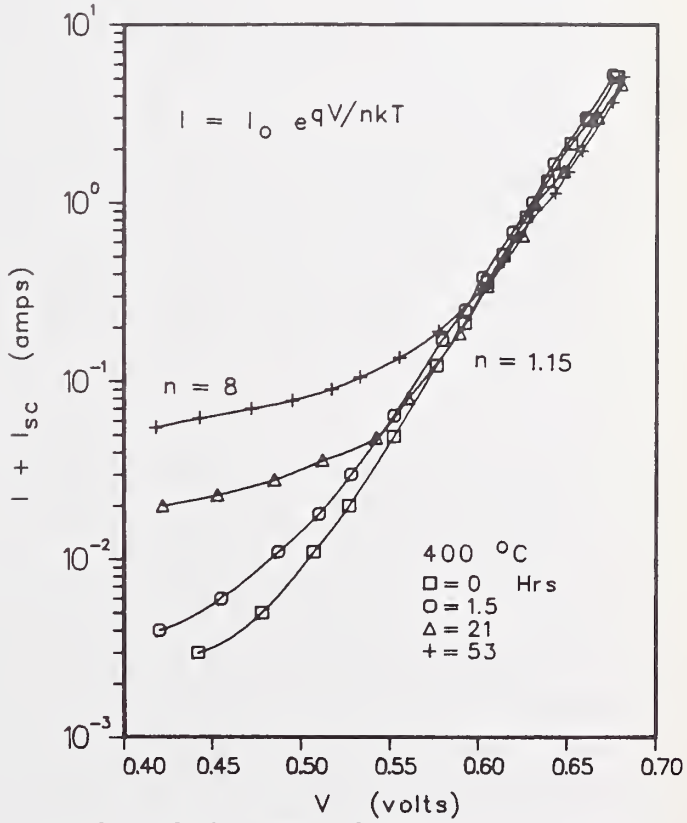


Fig. 3 Shifted current-voltage curves for a cell without Si_3N_4 encapsulation that was aged at 400°C in Ar for the times shown. Measurements were taken at an illumination of 100 mW/cm^2.

SOME RELIABILITY PROBLEMS IN INTEGRATED CIRCUITS - THEIR DETECTION, DEFINITION, AND REMEDY

by

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The predecessors of today's hand calculators, mini-computers, and main-frame computers were born at the beginning of the 1960 decade. Based on a 10 to 12 year foundation of steady progress in the development of bipolar transistors, integrated circuits (I/C's) developed at an even faster pace, with new logic families and new technologies, or major variations thereof, sometimes complementing, though more often superseding each other in meeting application needs.

This tutorial review is presented from the viewpoint of the end users of I/C's, the circuit designer and parts engineer, and is intended to alert their counterparts in a growing sister-technology of typical problems that the integrated circuit industry has encountered. Only a few of the many failure mechanisms known to have occurred will be reviewed, but these examples should illustrate the scope of the problems, which begin with device design, and continue through manufacture and test to end use by the buyer.

Some problems have been well understood and solutions have been readily adopted. In other instances, satisfactory solutions are lacking, not only where the problem is ill-defined, but sometimes even where characteristics and causes have been well-known for some time. In the latter case, manufacturers have often felt that corrective actions are not economically profitable, and high reliability users constitute such a small percentage (1 to 2%) of the total market that they can exert little pressure for modifications to manufacturing processes.

Reliability considerations gained new attention with integrated circuits, and stability of the devices has been and continues to be the prime barometer of device quality and reliability. Yet stability is largely a matter of definition. The obvious extreme case of instability is catastrophic failure of a device, i.e., when it fails to function at all. The more subtle failures are those of parameter degradation, wherein a parameter's absolute value changes to an unacceptable level, or where, even though the absolute level is not exceeded, the delta shift in a given time is excessive, with the probability that the parameter and device will continue to be unstable, and at some time exceed the parametric limit value. In the case of degradation, failures are sometimes defined in terms of a specific circuit application which dictates what is an acceptable limit; in

other circuit applications, the definition could be grossly pessimistic or optimistic. Electrical testing and simple tests easily identify most initial and early life failures. More insidious are those devices which give no early hints of eventual failure (or which we fail to recognize), but are placed in service and fail latently in situ. The most difficult challenge then is to define those environmental and operational stresses which accelerate degradation and catastrophic failure mechanisms, and implement practical procedures and tests to identify individual devices as good or bad.

Proper design of a device is clearly necessary in order to achieve the desired functional performance; it is also necessary in order to achieve the desired reliability. This is a paraphrase of the classical cliche in the semiconductor industry, that reliability can not be tested into a device - it must be built in. For example, the various transistors on an I/C die must be interconnected in order to perform the desired function. This is normally done by evaporating aluminum over the insulating surface, masking, and etching away to form the interconnection pattern. But since the aluminum is deposited over a topography which varies in elevation, voiding in the aluminum interconnect can occur where it passes over shoulders in the insulating glass surface (see Figures 1 and 2). Such voiding at these "steps" in the silicon oxide was a common problem in the semiconductor industry until 1971, when a Goddard Space Flight Center specification was issued which utilized a scanning electron microscope, with practical magnification capability of up to 40,000 X and a depth of field 30 times that of an optical microscope, to determine the quality of the metallization step at the very beginning of the manufacturing process. The use of such a sophisticated instrument on a manufacturing production line was revolutionary at the time, but is now an accepted, common procedure. The immediate and direct result of clearly identifying the problem characteristics at a point early in the manufacturing, when few dollars were yet invested in the product, was that most vendors made concerted efforts to modify their processes. One remedy was to slope the oxide step to a 45^{o} to 60^{o} angle (Figure 3). Others were to control substrate temperature, the use of planetary evaporation systems to reduce shadowing effects, etc.

One of the classical problems which was especially prevalent in the early and mid 1960's was "purple plague." This description was itself more colorful than accurate in describing the physical appearance of a failure mechanism which was due to the formation of intermetallic compounds. Gold wires had been - and often still are - used to electrically interconnect specific sites on the semiconductor die to the leads of the package in which the die is located. With improper processing (e.g., too high a bonding temperature, time and pressure, or too little aluminum), when the gold wire is bonded to the aluminum metallization, undesirable gold-aluminum compounds form which result in voiding at the interface, or which are brittle and make high resistance electrical contacts (Figure 4). Careful control of the

critical factors reduces such failures significantly, but most manufacturers instead chose to convert to a monometal system, whereby aluminum wire is ultrasonically bonded to the aluminum metallization on the semiconductor die (Figure 5). Here too, control of the process is necessary to achieve good bonds consistently.

In the assembly area, where semiconductor dice are electrically measured, bad ones removed and good ones mounted into packages, electrical connections made, and devices lidded, workmanship problems are especially severe because of the many cycles of handling by low and medium skill personnel. Automation reduces workmanship damage considerably, but does not eliminate it. A visual inspection of 100% of all devices just prior to lidding has been standard procedure for hi-rel devices from the infancy of I/C's. This "pre-cap" inspection by optical microscopes is done at 30X and 100X magnification, with many types of defects being addressed - scratches, voids, and smears in the aluminum interconnect (Figure 6), chemical contamination (Figure 7), and corrosion, improper bonds and bond locations, improper metal coverage at contact windows, improper lead positioning (lead dress) of wires from die to the package (Figure 8), detachment of dice from the package (Figure 9), particle contamination anywhere within the package cavity, diffusion and passivation faults, etc., etc. The military standard for this inspection, Test Method 2010 of MIL-STD-883, takes over 40 pages just to list and show line drawings of acceptance/rejection criteria. Where such inspections were practical yesterday with small scale integration (SSI) devices (Figure 10), and even medium scale integration (MSI) I/C's, it is not practical with today's large scale integration (LSI) (Figure 11). Where 10 to 20 transistors might comprise an SSI device, thousands exist on the same size (about 150 mil square) LSI, and the 10 to 15 seconds that an inspector might take to inspect 100% of the die surface at 30X or 100X for all acceptance criteria clearly is physically impossible. Proposed substitutes for pre-cap inspection, such as "high" voltage stressing have much merit for some types of faults, such as oxide and junction defects, but fail to address other types, such as scratches and poor alignment, adequately or at all.

During the assembly operations conductive particles can be introduced into the package. If they are only loosely attached at the beginning, they can break loose later in normal handling, during environmental testing, or in end use, such as the launch phase of a spacecraft. The number of sites even on a glassivated I/C die where a 2 to 4 mil conductive particle can short out two conducting elements (e.g., at the bonding pads of the I/C, or from lead to die edge - Figures 11 and 8), causing instant device and sometimes system failure, is unacceptably high. Yet unbelievably, 50 mil lengths of gold or aluminum wire have been found in devices which passed pre-cap visual inspection. Solder balls or weld splash from lid sealing, nickel flakes from lid platings, gold nodules formed during mounting of a die in a package, and even chips from the semiconductor dice themselves

- all are common sources of conductive particle contamination. As transistor and metal path geometries have shrunk with advancing technology, smaller and smaller particles can cause failures. Although this has been a moderate problem for 20 years, no general solutions in either product manufacturing or testing exist today which are 100% effective and economically practical.

Because of their small volume, low weight, and high packing densities achieved by their use, "flatpack" packages (Figure 12) are often used in spacecraft systems. But designers must learn how to properly handle these units, whose leads are typically about 15 mils wide and 4 to 5 mils thick. What would be normal handling for a transistor (with 25 to 30 mil diameter leads), if applied to a flatpack, would easily result in twisted, bent, or cracked leads, broken lead-to-package seals, dimpled lids, cracked ceramic, etc.

One recent package problem involved improper design and manufacturing of a particular style flatpack. External visual inspection of devices upon receipt from the manufacturer showed severe discoloration and microcracking where the lead was attached to the package (Figure 13). What appeared at first to be only a cosmetic defect - i.e., the appearance was bad, but no reliability hazard was evident - suddenly resulted in several packages each losing a lead (Figure 14). Failure analyses on the failed leads clearly showed corrosion products in the break (Figure 15). The culprit in the metallurgical construction of the leads was the existance of a nickel "barrier" metal between the base metal (Kovar) and the top plating (gold) (Figure 16). The nickel used here was electroless, very brittle and subject to microcracking under any handling whatsoever. The microcracks in the nickel underplate were visable through the gold overplate. Before the gold plating was applied, the nickel was subjected to a corrosive flux to suitably prepare the surface for the gold plating. This flux entered the microcracks and was plated over by the gold, in the process providing the electrolyte for a galvanic cell whose plates were gold and Kovar. On the failed devices and some others whose leads were sectioned, stress corrosion cracks propagated deep into the Kovar (Figure 17) at a point beneath a microcrack in the nickel plating. The use of ductile electrolytic nickel and proper plating procedures is the solution to this problem.

One hazard which extends over the entire gamut of manufacturing, test, and use in systems is that of electrostatic discharge (ESD). Insulated field effect devices, commonly called MOSFET's, are particularly susceptible to ESD, and precautions must be taken to provide handling safeguards. Workbenches with grounded, conducting tops, grounding straps for workers, conductive garments and floor pads, air ionizers, proper programming for test equipment, low voltage, grounded soldering irons or welding machines, conductive foam or packages for shipping, etc., are some of the necessary precautions. Yet ESD "ZAP's" still occur (Figure 18), most often caused by the end user with careless or

unthinking handling. The simple act of repackaging received devices in polyethylene bags after incoming inspection for distribution to individual users can be disastrous. For when that bag is opened, thousands of volts are generated and are available to damage the device as it is removed from the bag.

It should be evident to any user with a substantial interest and investment in a business utilizing I/C's, that the key word in the philosophy of operating is involvement. It is wrong to assign full responsibility for insuring the reliability of devices to a manufacturer and assume that he knows all about his own product, that he can and will investigate problems with your intensity of interest, and that he will give proper weight to your viewpoint. But involvement implies that users themselves must have a high degree of expertise in device design, processing and manufacturing, testing, and in specifying device requirements. It also implies a substantial investment of manpower and money to support those areas of expertise, and to perform product evaluations and failure analyses. Finally, it implies co-ordination and cooperation not only with other users, but certainly with manufacturers themselves, in order to promote some degree of standardization and to improve product reliability.

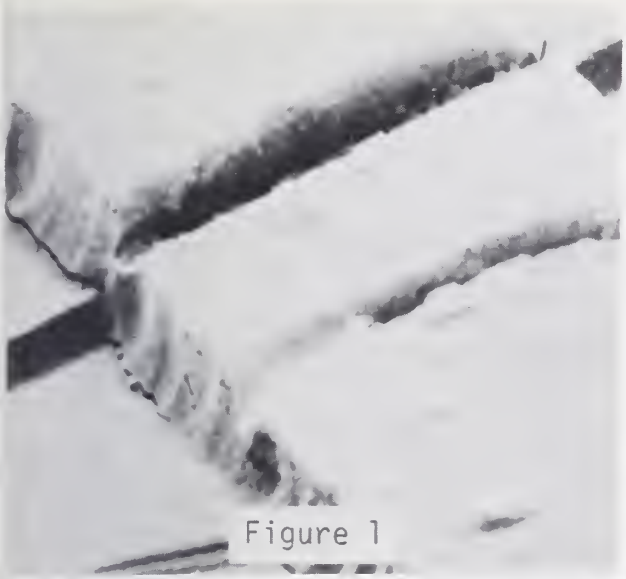

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Figure 3

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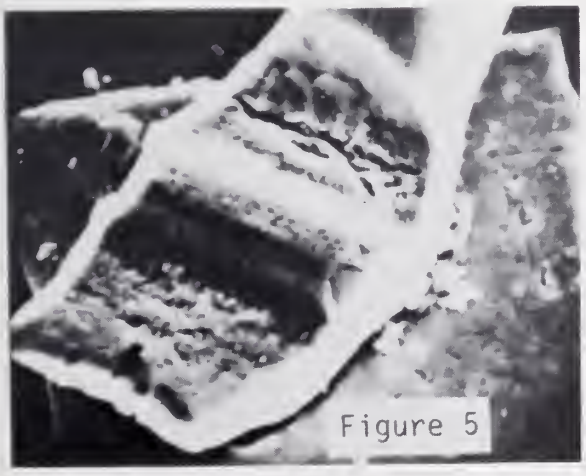

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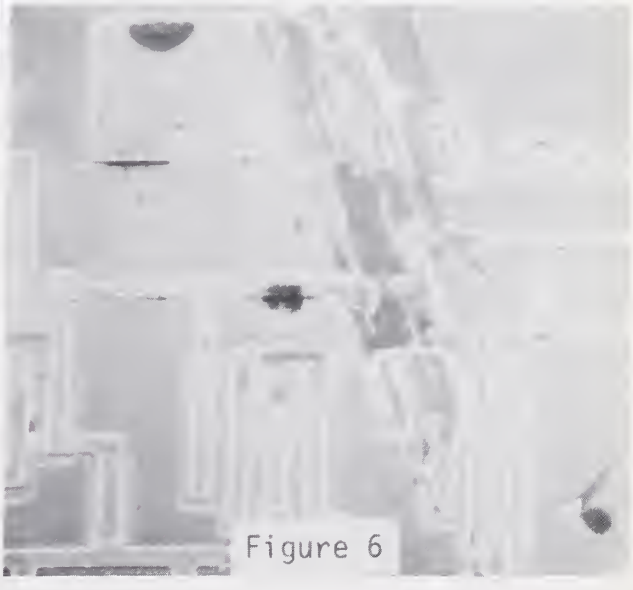

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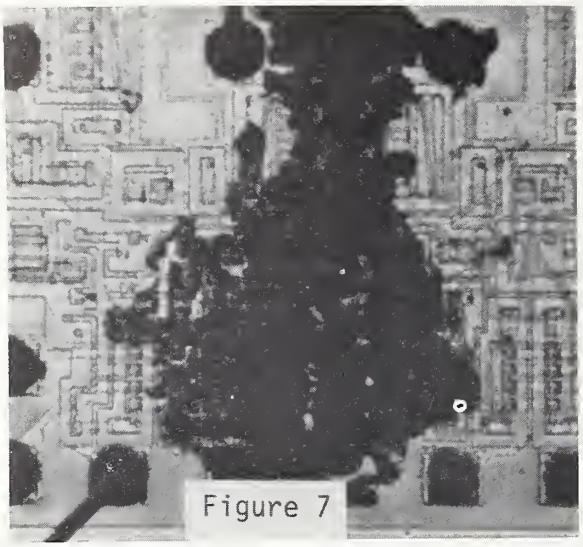

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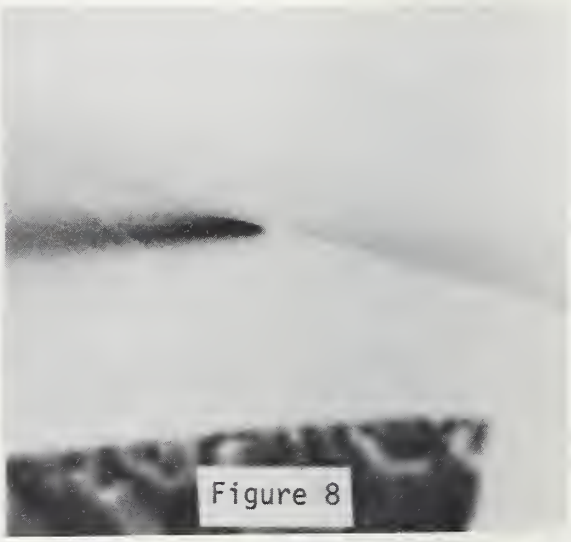

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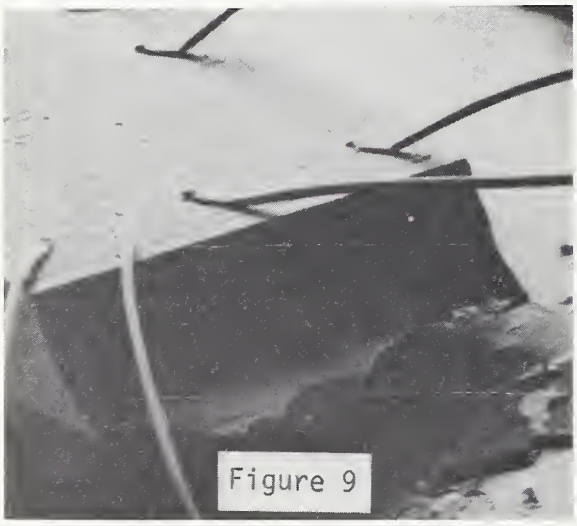

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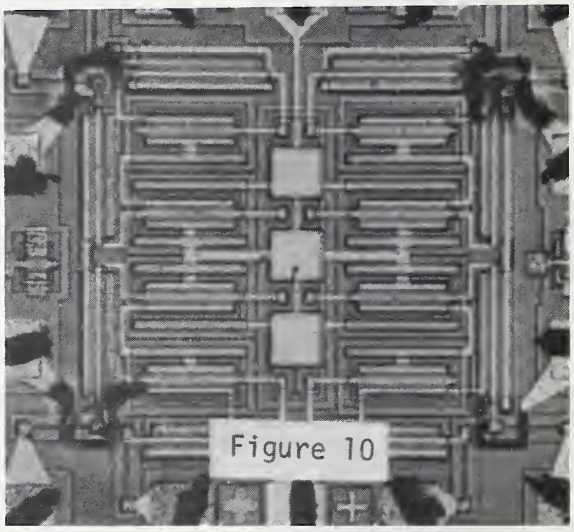

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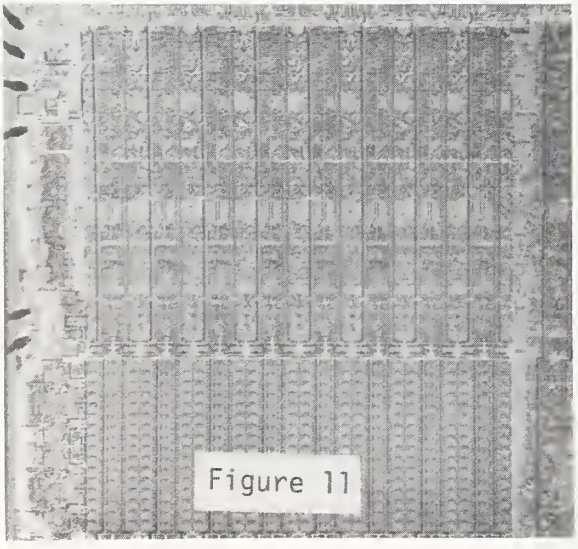

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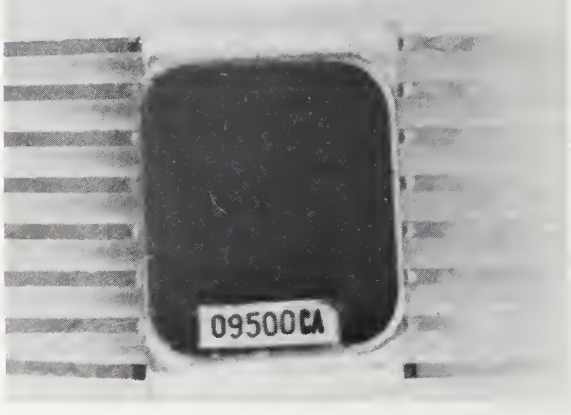
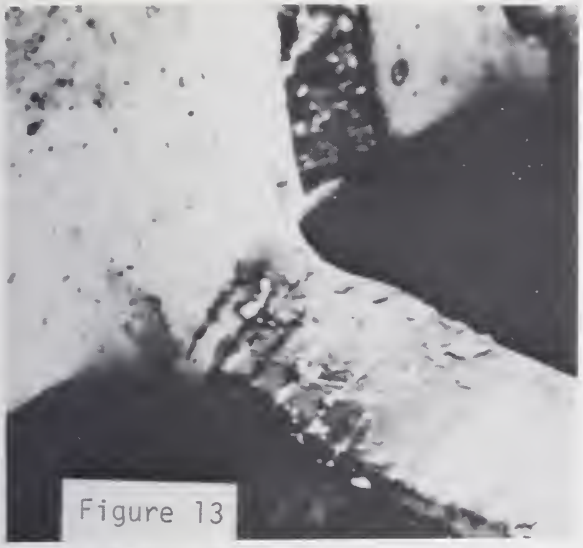
Figure 12





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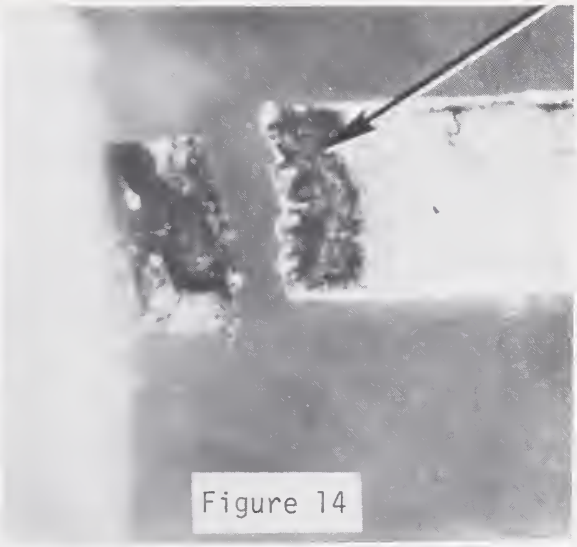

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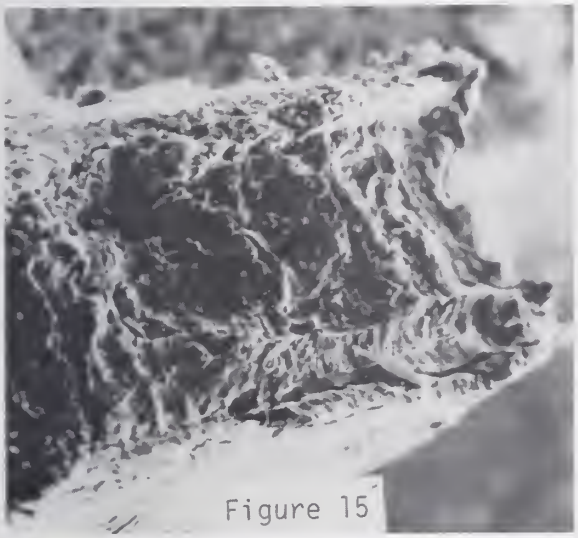

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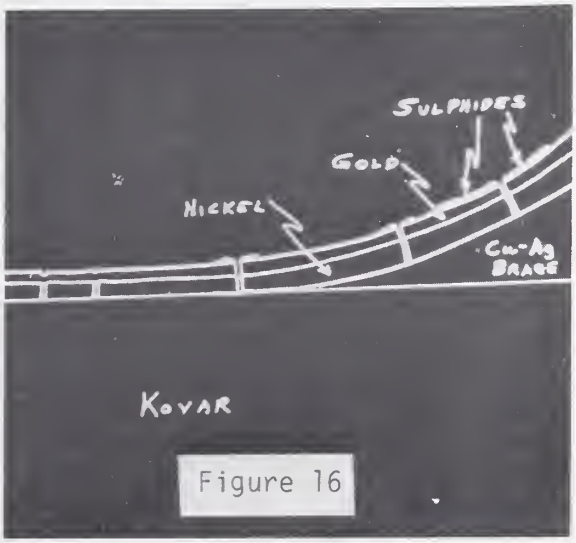

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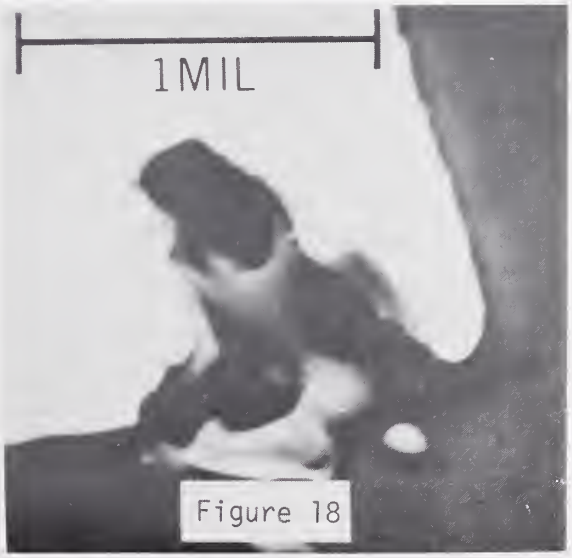

Figure 18

TESTS FOR INSTABILITIES IN SILICON INTEGRATED CIRCUITS

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Introduction

Silicon Integrated Circuits (SIC's), when properly designed, processed, packaged and screened, are generally stable and reliable devices having long-term failure rates of less than 100 FIT's* even for large, complex designs containing thousands of transistors.[1] However, there are many inherent drift and degradation phenomena which, with improper design or processing, can result in catastrophically high failure rates. The purpose of this paper is to briefly review the major SIC degradation and drift phenomena and the tests which can be used to uncover these mechanisms. For this purpose, the SIC is assumed to consist of a packaged silicon chip with the packaging material being an integral part of the device. Degradation and drift mechanisms associated with packaging will be treated first, followed by discussion of potential silicon chip instabilities. Emphasis is on tests which can uncover degradation and drift in completed product, but it should be recognized that more sophisticated analytical techniques are necessary to thoroughly understand and control the processing and materials parameters which permit these instabilities.

Packaging

While the silicon chips can be packed in various ways, the most popular packages are the dual in-line (DIP) ceramic with hermetic chip cavities sealed with metal lids or glass frits, and DIP plastic packages with the chip mounted on a metal lead frame and then molded in epoxy or silicone. The chip is bonded to the bottom of the ceramic cavity or to the metal lead frame "paddle" by various techniques including silicon-metal (usually Au) eutectic, epoxy paste (usually filled with Ag or Au) and low-temperature glass. Electrical interconnection between the chip and the package leads is usually by Al or Au wires, typically 1 mil diameter, with thermo-compression wedge or ball bonds. Problems specific to these DIP packages will be discussed, but similar problems can be expected with most SIC packaging techniques.

Let's first consider the interconnection function. Corrosion of external leads can cause open or high-impedance connections resulting in device failure. Usually the external leads are Kovar plated with Au, Ag, Ni, Sn or Sn-Pb solder, often with a flash of diffusion barrier metal such as nickel between the base metal and the surface plating. Accelerated life tests for terminal corrosion consist of high temperature[2] for intermetallic diffusion and phase transition,

*1FIT = 1 failure/10^9 device-hours

and temperature/humidity (perhaps in a corrosive atmosphere such as salt spray) for oxidation and electrolysis. Terminal shorts can occur as a result of metal migration, whisker growth and electrolysis. For Bell System applications, Ag is not allowed for terminal plating due to potential migration problems, plated Sn must be reflowed to prevent stress-induced whisker growth, and only Au plating is allowed for devices to be installed in sockets.

Internally, interconnection failures can be bond wire opens due to mechanical or thermal stress, high impedance or open bonds due to intermetallic diffusion, and open or shorts due to corrosion of bond wire or bond pad metals. In plastic encapsulated devices, the wires and the bonds are buried in the plastic and hence subject to stresses imposed by differential thermal expansions. These forces can pull apart weak bonds or plastically deform wires eventually causing fatigue failure. This is generally not a serious problem in epoxy-molded devices (where the plastic is in hydrostatic compression.)[3] In ceramic packages, the bond wires are suspended loosely between the two bond points. The wires can flex as a result of temperature changes or mechanical stress (shock, vibration, acceleration) and eventually fail through fatigue.[4,5,6] Such failures normally occur at the heels of bonds, particularly if the wire has been severely thinned or cracked during bonding. Perhaps the most infamous of the interconnection failure mechanisms is Al-Au metallic interdiffusion at the interface between the gold wire and aluminum bonding pads.[7] This temperature-accelerated phenomenon is characterized by progressive growth of various alloy phases and eventual bond failure through the development of Kirkendall voids,[8] but can be controlled by good bond quality unless aggravating factors are present. The degradation rate appears to be accelerated by certain contaminants (such as chlorine) around the bond area.

Electrolytic corrosion of the bond pads and bond wires can occur in the presence of moisture and a suitable electrolyte, particularly if some agent such as chlorine or phosphoric acid is available to reduce or penetrate the protective oxide skin on the aluminum.[9] Tests for interconnection stability include bond-wire pull tests and optical and SEM examination of bonds before sealing, high-temperature tests for intermetallic diffusion, temperature cycling or power cycling for plastic devices, and temperature cycling or power cycling followed by mechanical stress (centrifuge, shock, vibration) for ceramic devices. Evaluation of bond-wire pull strengths before and after sealing of glass-sealed ceramic devices (where sealing temperatures are quite high), or after high temperature exposure, can reveal potential intermetallic problems, but these are obviously destructive tests.

Ceramic packages depend upon hermeticity of glass or metal seals to protect the silicon chip from the external environment. Should the seals become leaky, water vapor and contaminants can enter the package cavity. In the glass-sealed packages, the metal lead frame is

usually sandwiched between ceramic layers cemented by a glass frit which encompasses the metal leads. Thus forces on the package leads are amplified by mechanical advantage to the glass frit, and can often crack weak glass seals. The solder seal for metal lids can be stressed to failure by differential temperature expansions of the metal lid and ceramic base. Tests for package integrity, then, consist of temperature cycling or thermal shock for both glass and metal sealed packages, lead bending and straightening tests for both glass and meta devices, and fine and gross leak checks.[10,11] Fine leak testing is performed with pressurized helium or radioactive Krypton. Gross leak testing is best done by pressurizing the devices in a fluorocarbon bath, then boiling off any entrapped fluorocarbon in a bubble chamber (MIL 883A, Method 1014.1, condition C).

All plastics are permeable to water to some degree, so plastic encapsulations offer only limited protection from external environments.[12] Water molecules eventually penetrate the plastic to the chip surface, along with ionic contaminants from the external surface or from the plastic material itself. The effects of the water and contaminating ions on chip operation depend strongly on the lateral mobility of ions along the chip surface, which depends in turn on the adsorbed water layer being continuous. Therefore, the moisture protection provided by the plastic encapsulant depends on the adherence or the chemical affinity of the plastic to the chip surface. Various tests are used to evaluate the susceptibility of plastic devices to water. For completed devices, probably the most effective test is biased temperature-humidity, where the device is biased with operating voltages for minimum power dissipation in an ambient, typically, of 85°C/85% R.H. Plastic materials tests include measuring the weight gain of the absorbed water in high humidity and aqueous extraction evaluation of hydrolized ionic contamination levels.

Some plastics, particularly the epoxies containing flame retardants, can release relatively large amounts of halides (bromine and chlorine) at high temperatures.[13] These free halides can attack bond wire and chip metallization, and appear to be responsible for catastrophic failure of Au-Al bonds observed in a few hundred hours at temperatures as low as 150°C. Activation energy for this phenomenon seems to be about 1 eV, so the problem could be significant for plastic-encapsulated devices operating at high temperature.

Another primary function of packaging is heat dissipation. In the standard DIP package configurations, most of the heat is removed from the chip via the die (chip) bond. Voids or cracks will increase the die bond thermal resistance and hence increase chip temperature.[14] Voids can sometimes be detected by transmission Xray, by ultrasonic techniques or by visual inspection of the chip periphery. Cracks can be induced by temperature cycling or thermal shock and poor bonds can sometimes be screened out by centrifuge. Poor thermal conductance

can be evaluated by making thermal impedance measurements - a slow and expensive procedure which is not practical for 100% screen testing.

Another factor which can be detrimental to long-term SIC reliability (and which has begun to receive a great deal of attention) is water vapor and other gaseous products sealed into the cavities of hermetic packages.[15] This can obviously be as harmful as water ingressing from the external atmosphere. With reasonable attention to preseal drying and control of the sealing atmosphere, the humidity in metal-sealed ceramic packages should be well below 1000 ppm (volume). Moisture in cavities of glass-sealed devices, and those with glass or epoxy die bonds, may be much higher due to moisture outgassed during sealing or evolved during cure. Moisture in the package cavity can be measured directly by puncturing the cavity in special mass spectrometer apparatus, but this is a destructive test. Dew point measurements have been made on some devices, but are not generally practical. Special moisture sensors inside the cavity have also been used, but with a few exceptions, such sensors are mainly useful for process control and would not be encapsulated in every device. Another technique used to determine susceptibility of devices to cavity moisture is to operate the devices at $\sim$0°C[16], or to operate the devices as temperature is cycled a few degrees above and below 0°C for several hundreds of hours. While this low-temperature operating test has been successful in showing that entrapped water can indeed cause device problems, it is unlikely that such a test would be sufficient proof that a device would not be susceptible to entrapped water.

Silicon Chips

Silicon Integrated Circuit chips essentially consist, from the top down, of glassivation, one or more levels of interconnection metallization, one or more layers of dielectric insulation and then silicon doped with impurities in various and sundry ways. Each of these are subject to instability mechanisms which can influence the stability of the device.

Glassivation

"Glassivation" is a protective covering which, in itself, should not contribute to the operation of the SIC. However, it can contribute to (or detract from) the stability of the device depending upon its ability to protect the underlying materials from water and contamination. While various inorganic and organic materials have been used for surface protection, the three most common materials currently used in commercial SIC's with aluminum metallization are low-temperature vapor deposited glass (vapox), vapox with phosphorus, and plasma-deposited silicon nitride. Vapox, being porous, is always permeable to moisture, but its moisture protection capability is often further degraded by voids and cracks. Vapox with phosphorus is easier to deposit uniformly, and, if the weight-phosphorus content is within the range of about 1 to 4 percent, can provide protection as well as sodium ion mobility.

However, if phosphorus content exceeds about 4%, there is an apparent phase separation into a hygroscopic P_2O_5 constituent which allows rapid water absorption in the film.[17] The dissolved P_2O_5 can form phosphoric acid which reduces aluminum oxide and thus allows corrosion of the underlying aluminum metallization. Plasma deposited silicon nitride seems to be a good barrier against both water vapor and sodium, but is difficult to deposit without cracking. For packaged devices, there is no straight-forward test for glassivation integrity; but the relative quality can be judged by visual inspection, measuring the phosphorus content using an electron or ion microprobe, and measuring the thickness and feature coverage after cross-sectioning. Of course, glassivation quality may show up indirectly in the results of temperature and humidity life tests on the device.

Metallization

Most commercial SIC's use aluminum metallization for interconnection of circuit elements. Other metal systems such as Ti-Pt-Au for beam-lead devices and Ti-W-Al for Schottky-clamped devices with platinum silicide contacts are also in wide usage. This discussion will primarily concern aluminum metallization. Basically the process consists of evaporating the aluminum over the entire surface of the device, then patterning the aluminum using standard photo-resist and chemical etching procedures and finally sintering at about 500°C to form ohmic contacts where the aluminum directly contacts the silicon. Major failure mechanisms include corrosion,[18, 19, 20] cracking, metal electromigration[21, 22] and silicon diffusion and electromigration.[23]

A thin layer of stable oxide forms rapidly on aluminum exposed to air. This oxide protects the aluminum from corrosion. However, this oxide layer can be breached by contaminating ions such as chlorine, allowing rapid corrosion by reaction of the exposed aluminum with water. Such reaction is independent of electrical bias, but if bias is applied, the chlorine ions are attracted to the anode - thus the positively-biased metal lines will corrode preferentially. As mentioned in the previous section on glassivation, aluminum corrosion can also be accelerated by phosphorus leached from doped oxide insulator layers. Phosphorus-related corrosion apparently involves the generation of negative hydroxyl ions at the cathode which react with the aluminum; the phosphorus probably serving to break down the protective oxide and as an electrolyte. This reaction occurs preferentially at aluminum grain boundaries so that very little of the aluminum need be converted to create high impedance or open electrical paths. Biased temperature-humidity life tests are effective for uncovering corrosion problems in plastic packages. It is likely that halogens released at high temperature from flame retardants in plastics will also accelerate corrosion failure. Analysis of vapox indicating more than 4% phosphorus or of underlying thermal oxides indicating more than 8% phosphorus should be cause for concern. Cracked glassivation is also a possible

metal corrosion accelerator since capillary condensation can allow liquid water in fine cracks down to the metal surface, even at relatively lower ambient humidities.

Evaporated aluminum films are subject to cracks from a number of causes. First, these films are under tensile stress as deposited so cracking can be a stress relief mechanism. Cracking of this nature is most likely at the edges of sharp vertical features such as contact windows, where the aluminum can be much thinner (and stresses much higher) than on flat surfaces. Another possible cause of cracks is silicon precipitation at aluminum grain boundaries causing embrittlement and subsequent cracking under thermally induced stress. Finally, fatigue cracking can develop as a result of thermal cycling. Thermal fatigue cracking is preceded by surface reconstruction[24] involving formation of hillocks and ridges over the aluminum surface. The most effective tests for metal cracking are temperature cycling and power cycling.

Electromigration is mass transport due to electric current. Circuit failure results from local depletion of metal at grain boundaries or points of high current density such as thinned spots or around voids. This phenomenon begins to be a problem in thin aluminum films at current densities of about 10^5 amps/cm^2. The rate of degradation has been observed to have an activation energy of .5 to 1 eV, and to be proportional to between the second and fourth powers of the current density.[25]

High current tests for electromigration are often impractical for packaged devices because the problem is likely to occur at anomalous defects buried in the chip circuitry. In some cases potential problems can be accelerated by testing at high temperatures and currents. If resistance of individual lines can be precisely measured, the rate of resistance change with fixed current can be used to predict time to failure. In any event, it is very important that the device design assure average current densitities well under 10^5 A/cm^2 with minimum widths and thicknesses.

Silicon-aluminum interdiffusion can cause a number of different problems. Diffusion of silicon into aluminum metallization in contacts can cause electrical opens due to the formation of Kirkendall-type voids. The silicon diffusion rate is accelerated by electrical current through electromigration. These phenomena can create etch pits preferentially at silicon crystal defects, allowing aluminum to migrate through the etch pits in shallow junctions and short-circuit the metal to the silicon substrate. Silicon in the aluminum tends to precipitate at aluminum grain boundaries, causing high electrical impedance, embrittlement and loss of inter-granular cohesion. Most of these interdiffusion problems can be minimized by using saturated Al-Si alloy. High temperature, high current (when feasible) operating tests are probably most effective for detecting silicon-aluminum interdiffusion problems in packaged devices.

Dielectric Insulators

Insulation layers play a very important role in the operation of SIC's. Their function obviously includes electrical insulation between metallization layers and between metallization and silicon. But they must also assure that electrostatic fields cannot invert the silicon surface between circuit elements. In MOS devices, the characteristics of the gate insulator determine the critical transistor threshold voltage. Instability mechanisms in dielectric insulators include mobile ion drift,[26] interface charge trapping,[27] bulk charge trapping,[28, 29,30] field-induced polarization,[31,32] surface charge migration and dielectric breakdown.[33,34,35] SiO_2, which is the primary insulator used in SIC's, is chemically stable, has very high electrical resistivity and good breakdown characteristics and has very low density of trapping centers and active Si-SiO_2 interface states. Due to its relatively open structure, however, contaminating ions such as sodium are quite mobile in SiO_2, and can move rapidly through the oxide to the silicon interface. This mechanism, in fact, has been historically the bane of the semiconductor industry and, in spite of many process and design innovations to combat the problem, may yet be the single most important instability in SIC's. Sodium ions at the Si-SiO_2 interface cause several device problems, the most important being the tendency to invert P-type surfaces to create conducting channels between circuit elements and to modify transistor threshold voltage of MOS devices (decrease N-channel thresholds, increase P-channel thresholds). The postive sodium ions can decrease junction breakdown voltage and increase leakage by field enhancement and by creating field-induced junctions. Sodium also can lower SiO_2 breakdown strength by reducing the barrier for electron injection from the silicon into the oxide.

In addition to using cleaner chemicals and facilities, processing innovations to reduce sodium drift problems include the introduction of HCL in the oxide growth process to chemically neutralize sodium at the silicon interface, and the use of multi-layer dielectrics to getter sodium introduced from previous process steps and to inhibit sodium mobility toward the silicon. Examples of multi-layer dielectrics used for these purposes are Si_3N_4 over SiO_2 used as a sodium barrier in the Bell beam lead-sealed junction devices, and phosphorus-doped glass (PSG) over SiO_2 used in most commercial SIC processes. While both Si_3N_4 and PSG are effective in reducing sodium drift, they can introduce additional problems and must be applied with discretion.[36] Both PSG and Si_3N_4 polarize readily, and both contain much higher densities of trapping centers than SiO_2. Further, lateral charge migration can cause device problems with these materials since the bulk resistivity of Si_3N_4 is generally much lower than that of SiO_2, and for PSG layers, charge can migrate along the PSG-SiO_2 interface. Polarization, charge trapping and bulk and interface conductivity all contribute to time-varying electric field intensity gradients in the underlying SiO_2 and hence at

the silicon surface. In the field regions between devices, the SiO_2 should be sufficiently thick to protect against surface inversion regardless of the overlying PSG or Si_3N_4 characteristics. Great care should be taken in using these materials in the thin gate oxide regions of MOS transistors. In particular, the PSG or Si_3N_4 layer should be located adjacent to the gate metal, and thickness should be very much less than the thickness of the SiO_2 layer to minimize threshold drift.

Comprehensive tests for sodium contamination in complex SIC's are very difficult to devise because sodium drift is so dependent on local concentrations and fields and its effect on device operation occurs only after sufficient accumulation to cause surface inversion or dramatic changes in threshold or breakdown voltage. Biased high-temperature testing is the only practical means for detection in the packaged devices. If sodium is the culprit, drifty devices can often be recovered by annealing at high temperature without bias. This thermally reversible drift effect is often cited as evidence of sodium contamination even though similar failures for other causes (e.g., polarization, charge trapping, radiation ionization) may also be reversible. Since it is so difficult to reliably assess ionic contamination in complex devices, high temperature C-V measurements on MOS capacitors or V-I measurements on MOS transistors are often used, particularly for process control.

$Si-SiO_2$ interfaces contain charge trapping sites which are centers with energy levels in the silicon band gap and which can exchange charge with the silicon. This means that charge can accumulate at the surface depending on the electrical field at the surface and the density and energy states of the centers. Interface state density is strongly influenced by processing and by crystal orientation (larger for 111 orientation, smaller for 100 orientation). Interesting properties of interface traps are that (1) traps near the middle of the silicon band gap act as recombination-generation centers which increase junction leakage and flicker noise; (2) trapped charge tends to compensate the applied field, resulting in lower fields at the silicon surface and (3) the interface charge changes with time, temperature and applied field, resulting in long-term drift at normal operating conditions. Perhaps the most significant effect of this drift in actual devices is the potential for an increase of several tenths of a volt in the threshold voltage of P-channel MOS devices (processed on 111-silicon) over the expected life of the devices. Biased high-temperature life tests are useful for evaluating interface trapping effects in actual devices, but C-V measurements on MOS capacitors yield much better insight into the characteristics of the phenomenon.

Charge trapping in the bulk of the SiO_2 near the silicon surface is another source of problems in SIC's. Trapped charge may be either positive or negative, and the effects on device operation are similar to those of other charges (such as sodium or charged interface trapping centers) located near the silicon surface. Energetic charges having

energy greater than the $Si-SiO_2$ interface barrier potential can move from the silicon into the SiO_2 and become trapped near the silicon surface. This effect becomes significant when there is a high normal field component to accelerate the charge toward the oxide, and when there is a large source of free charge near the silicon surface as from junction avalanche breakdown, impact ionization near the drain in MOS transistors operated in saturation, or junction leakage current at high temperatures. Trapped negative charge due to "hot" electrons probably creates more actual device problems than positive charge because the barrier potential is higher and mobilities lower for holes than for electrons. Trapped injected charge has been shown to affect the operation of MOS and bipolar devices, and is responsible for "walk-out" of gate-controlled diodes.

Another mechanism for oxide charging is radiation ionization,[37,38] where the radiation creates a net positive charge in the oxide, thus increasing inversion threshold for P channels and decreasing inversion threshold for N-channels. While radiation exposure is an interesting tool for evaluating device margins by varying threshold voltage, this should not be a problem for SIC's in a normal terrestrial environment.

Dielectric breakdown, particularly in thin gate oxides, is one of the dominant failure mechanisms in MOS devices. Breakdown is a local high-current occurrence which can be self-healing in some cases, or can become a permanent short circuit through the oxide, depending on the gate metallization, circuit impedances, etc. Although breakdown probably occurs at defects or weak spots in the oxide, the critical externally-applied electric field varies with time. This time-dependent breakdown threshold field (or gate-to-silicon voltage) likely results from variations of charge within the oxide causing local field enhancement and hence avalanche breakdown. Mobile sodium ions and trapped holes or electrons can cause such field enhancement within the oxide itself. MOS devices are often stressed at voltage levels much higher than normal operating voltage levels to weed-out early gate oxide breakdown failures. High temperature is also effective to some degree, since the activation energy of this failure mechanisms appears to be about 0.3 eV.

Lateral charge migration along surfaces of dielectric insulators can create time-dependent device problems due to leakage at circuit nodes or to silicon surface inversion between circuit elements. The latter is particularly insidious when thin spots or holes in the field oxide exist in areas not covered by metal. Time to failure is then dependent on surface impedance or interface charge diffusion characteristics. For very dry hermetically sealed devices, biased high-temperature testing may be most effective for weeding out such problems. On the other hand, if enough water vapor is present in the package cavity, biased testing at temperatures near the internal dew point should accelerate surface charge migration via adsorbed surface water. For this reason, biased temperature/humidity testing may be most effective for plastic devices.

Silicon

The silicon crystal structure and diffused or implanted dopant profiles are quite stable in typical SIC's operating at normal current densities and junction temperatures. This is not necessarily true of other semiconductors such as power switching transistors and microwave devices [39,40] where local hot spots may cause extensive changes in the silicon crystal structure, or in photo-optical devices such as heterojunction lasers[41] and light-emitting diodes where the growth of crystal defects can drastically effect device operation. For SIC's, however, the only significant problem with the silicon is the growth of cracks as a result of stress relief, thermal stress or mechanical stress. The most effective tests for silicon cracking are probably temperature cycling and power cycling.

Other Failure Mechanisms

The SIC failure mechanisms discussed herein generally constitute relatively slow processes under normal operating conditions. However, severe overstress (such as electrostatic discharge) can result in more or less instantaneous failure due to other mechanisms such as metal fusion, silicon melting, etc. And, for complex LSI devices, apparent failure in system usage can be simply due to insufficient electrical testing at the device level.

Conclusion

The major degradation and drift mechanisms in silicon integrated circuits are time-variant charge distributions affecting the electric field intensity and energy states at the silicon surface, and various phenomena affecting the electrical continuity and isolation of metal and silicon. These may result in device malfunction at any time depending upon the unique characteristics of the individual devices as well as the features of the general population. A small percentage of devices can be expected to fail in early life due to processing anomalies which cause particular sensitivity to a failure mechanism, whereas the remainder of the population may not be afflicted until much later (if at all). Most of the instabilities are functions of electrical bias, humidity, temperature or temperature excursions, and can be accelerated by application of extraordinary values of these parameters. Thus these parameters can be useful for evaluating the stability of packaged devices and for screening out weak units within times much shorter than the expected life of the devices under normal conditions. Tables 1-4 summarize the type of tests expected to be useful in identifying devices afflicted by the various drift and degradation mechanisms. References 42 & 43 discuss techniques for using accelerated life test data to predict failure rates under normal operating conditions.

In complex large-scale integrated (LSI) devices, it is impractical to apply worst-case conditions at each circuit element and to quantify the rate of drift or the extent of degradation prior to device failure. Accelerated-life testing of LSI devices is at best only partially successful and relatively gross. Such testing must be complemented by thorough analysis of device failures and evaluations of the device fabrication materials and processes in order to achieve sufficient insight into device quality and reliability. Procurement specifications for SIC's purchased for Bell System applications require accelerated life testing of representative samples for shipment qualification. In addition, samples of devices are periodically evaluated by Bell Labs to assure that changes in design or processing have not occurred which could adversely affect device reliability but escape the specified shipment qualification tests. Laboratory evaluation includes more extensive accelerated life testing as well as rather thorough analysis of packaging and chip processes and materials. If good process and materials practices are observed, and if the devices perform well under accelerated-life conditions, it is likely that the SIC's will be stable during long field service.

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TABLE 1
ACCELERATED LIFE STRESS TESTS FOR SICS

Test	Conditions	Purposes and Limitations
HTB (Static) (Hi Temp.Bias)	150-250°C Max Voltage Fixed Input States	Surface & bulk charge migration, metal & silicon electromigration, interface & oxide charge trapping, intermetallic diffusion, oxide breakdown (Some elements not biased Worst-Case)
HTB (Dynamic) (Hi Temp., Bias)	125-200°C Max. Operating V: Varying Input States	Generally same as HTB (Static) Advantages: Necessary for "dynamic" and "bootstrap" circuits; exercises all internal nodes Limitations: Average $\bar{E}$ field may not be worst case.
LTB (Lo Temp,Bias)	$\leq$0°C Max. Voltage Dynamic or Static	Internal condensation for metal corrosion surface conductivity. Also may be worst case for charge injection and trapping.
HT (Storage)	200-350°C No Bias	Intermetallics & other diffusion mechanisms. Temperature not limited by device operation.
T/H/B (Temp/Hum/Bias)	85°-150°C 80%-100% R.H.	Electrolytic corrosion, surface charge migration, hydrolysis of contaminants. Effective for plastic and epoxy-sealed packages; only affects external pins on metal or glass sealed devices.
T.C. (Temp.Cycle)	$\sim$50°C to + 150°C No Bias	Fatigue of package seals, bond wires die bonds, wire bonds, chip metal, etc.
P.C. (Power Cycle)	Power On-Off Max V,I	Fatigue and stress due to local thermal gradients not possible with temp. cycling. Effective for high-power types. For best effect, power transients should be very fast.
Mech.	Centrifuge (20KG-30KG) Shock (3KG-20KG) Vibration (20G-70G)	Mechanical stressing of wire and die bonds. Centrifuge probably most effective for SIC's in ceramic packs.

TABLE 2
SIC INSTABILITIES

Packaging

Fault	Cause	Accelerating Factors*	Tests**
Pin Corrosion	Intermetallics	T, C	HT, HTB
	Oxidation	T, H, C	HT, HTB, T/H/B
	Electrolysis	T, H, B, C	T/H/B
Open Bond Wire	Break	M	Mech
	Fatigue	ΔT, ΔM	T.C., Mech
	Intermetallics	T, C	HT, HTB
	Corrosion	T, H, B, C,	T/H/B
Broken Die Bond	Stress Crack	ΔT, M	T.C., Mech., P
Water Ingress	Permeation	T, H	T/H/B
	Leaks	ΔT, M	T.C., Lead Ber + Leak Tests
Contamination (Plastics)	Hydrolysis	T, H	T/H/B
	Decomposition	T	HT, HTB

* T: Temperature ΔT: Temp. Change H: Humidity
B: Bias C: Contamination M: Mechanical Stress
ΔM: Mechanical Stress Cycling

**See Table 1 for definitions of abbreviations

TABLE 4
SIC INSTABILITIES

Chip Metal

Fault	Cause	Accelerating Factors*	Tests**
Opens or High Impedance	Stress Relief	ΔT	T.C., P.C.
	Fatigue	ΔT	"
	Surf. Reconstruction	ΔT	"
	Si Precipitation	ΔT	"
	Metal Electromigration	T, I	HTB
	Si Electromigration	T, I	HTB
	Chemical Corrosion	T, H, C	T/H
	Electrolytic Corrosion	T, H, B, C	T/H/B
	Intermetallic Diffusion	T	HT, HTB
Shorts	Electrolytic Migration	T, H, B, C	T/H/B
	Metal Electromigration	T, I	HTB
	Junction Penetration	T, I	HTB
	Whiskers	T, H, B	T/H/B

TABLE 3

SIC INSTABILITIES

Dielectric Insulators and Silicon

Faults	Cause	Acceleration Factors*	Tests**
Si Surface $\overline{E}$:			
(Surface inversion MOS threshhold shift, junction breakdown, junction leakage)	Mobile ions in SiO_2	T, B	HTB
	Surface Charge Migration	T, H, B	T/H/B
	Interface Charge Migration	T, B	HTB
	Interface Charge Trapping	T, B	HTB
	SiO_2 Charge Injection	B, T?	HTB, LTB
	Polarization	T, B	HTB
	Radiation Ionization	T, B	HTB, HT

*See Table 2 for abbreviations

**See Table 1 for abbreviations

Real-Time Controls for Reliability Assurance

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The accumulation life-test data under conditions that are application oriented to obtain mean-time-to-failure (MTTF) data is an oversimplified way of demonstrating reliability when one desires millions of device hours with a small number of failures. Unless one is interested in demonstrating only modest levels of reliability, this procedure will be totally inadequate for determining how well the manufacturing process produces devices that meet the intended design criteria. Table I indicates the enormous sample sizes required to demonstrate very low failure rates. The equally enormous expenditures in facilities and time required to test samples of the sizes shown is obvious.

The classical approach to reliability testing was developed years ago because some overall protection in the form of reliability assurance was needed by customers. This testing, performed under standardized MIL-STD-883 conditions, was necessary and useful. Reliability engineers overstress-tested devices to destruction and built a foundation of knowledge. A wealth of customer field information also became available. Failure analysis performed on a routine basis added even more knowledge. The net result was and is a greater understanding and appreciation of categories of potential failure mechanisms associated with different product designs than was previously possible.

Real-time control testing is an important supplement to the traditional approach to reliability assurance. Its basis is the use of accelerated testing where the level of stress is knowledgeably selected to maximize the acceleration of useful life. The key is in selecting as large a stress level as possible without activating failure mechanisms that are not active during the operational life of the devices being tested. That this selection can be done with assurance is based on the information bank accumulated by the traditional efforts in life testing, stress testing, failure analysis, and field use.

The advantage of real-time control testing is that device analysis can be accomplished quickly and with few samples. Very often a two- or three-day accelerated life test can be used to predict the performance of a product in an actual-use application over a five- to seven-year period.

The first real-time control was developed to control the thermal-cycling capability of silicon power transistors in plastic packages.[1] More recently it has been successfully used to assure the reliability performance of COS/MOS integrated devices.[2] For the details of real-time control testing the reader is asked to refer to the references cited and those that are cited therein.

Table I - Sample Size Required for 1000-Hour Life Test

Failure Rate % per 1000 h	With Zero Failures at 90% Confidence	With One Failure at 90% Confidence	With Three Failures at 90% Confidence
1.0	231	390	668
0.1	2,303	3,981	6,681
0.01	23,026	38,980	66,808
0.001	230,000	389,000	668,000

[1]Gallace, L. J., and Lukach, V. J., Real-Time Controls of Silicon Power-Transistor Reliability, RCA Application Note AN-6249, February 1974.

[2]Gallace, L. J., and Kukunaris, S., Reliability Real-Time Controls of COS/MOS IC's, RCA Publication ST-6709, January 1978.

INTERDIFFUSION AND INTERFACE PROBLEMS RELATING TO THIN FILM PHOTOVOLTAIC DEVICES

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Even a cursory examination of the cross-section and microstructure of a thin-film polycrystalline solar cell can produce some skepticism in the mind of the most ardent thin-film photovoltaics advocate. How can this device, with its maze of grain boundaries, interfaces, defects, surfaces, and metallurgical junctions, be expected to remain reliable or stable even if it is allowed to remain unmolested let alone exposed to severe fields, illumination, changing loads, temperature gradients and cycling, and its entire processing sequence. In fact, the challenge of stability assurance over 10-20 year time periods is equally if not more important to the photovoltaic effort than the 10% efficient thin-film device or the $0.50/peak watt program goals. This paper focuses on potential and real problems relating to the interaction of the materials making up the solid state devices and compounded by the special considerations of thin layers of polycrystallinity.

I. THE PROBLEMS--IN GENERAL

A simplified but illustrative representation of a thin-film device is shown in Figure 1. For the purposes of this paper, the major problem areas indicated are primarily considered. They are: a, the grid or finger contact/semiconductor interface; b, the semiconductor/semiconductor (or junction) interface; and c, the semiconductor/back-contact region. a', b', and c' represent the special cases of a, b, and c at grain boundaries where enhanced interactions can occur.

The movement of atomic species, or the diffusion mechanism, is prevalent to some extent in all solids and materials systems. Basically, diffusion can be defined in two identifiable regimes: (1) Diffusion in a material at chemical equilibrium. That is, there exists a uniform chemical and native defect composition. For the solvent species, the process is called SELF-DIFFUSION, and for the solute species, ISOCONCENTRATION DIFFUSION; (2) Diffusion entailing a net chemical flux. In this case, the system is not in equilibrium, and the resulting chemical potential gradients establish chemical fluxes. This chemical diffusion or INTERDIFFUSION results in the net flow of matter which generally leads to an expansion (but sometimes a contraction) of the diffusion region. This is illustrated in Figure 2. At $t = 0$, the materials are brought into contact, some atomic interarrangement occurs for $t > 0$, and equal distribution is reached at infinite time. The term "interdiffusion" is usually applied to any case when atomic

interpenetration is experienced after metallurgically coupling two materials. This penetration can be significantly enhanced along defects, such as grain boundaries. The interdiffusion problem and its effects on device stability form the major considerations of this paper. In addition, some other interface problems which limit device performance and result from device processing are discussed. Representative examples are cited from a variety of device types including SnO_x/Si, CdS/$CuInSe_2$, CdS/$CuInS_2$, CdS/$CuInTe_2$, Cu_2S/CdS, InP/CdS, GaAs, and amorphous Si.

II. THE TECHNIQUES--AES AND SIMS

The diffusion process has been studied, simplified, complicated, interpreted, and misinterpreted using a variety of techniques. The relatively recent development of surface analysis techniques which can provide elemental and chemical information about fraction of monolayer thicknesses has been important to both the uncovering of diffusion-related problems and the investigation of the mechanism itself. Of the more than 60 identified surface measurement techniques which have been reported,[1] two which are complementary in nature have highlighted interdiffusion investigations: (1) Auger electron spectroscopy (AES); and (2) secondary ion mass spectroscopy (SIMS). The AES technique analyzes Auger electrons generated by a radiationless process by an incident electron beam. SIMS, on the other hand, uses an ion probe to give rise to secondary positive and negative ions from the material under investigation. Detailed information about these techniques is available in the literature[1] and therefore, will not be discussed herein.

Application of the AES technique in combination with ion etching to diffusion problems and extensive interpretation of the results has been reported by Morabito and Hall for single crystal (bulk)[2] and grain boundary[3] cases. Their formalism, which is equally applicable to SIMS, extracts the bulk interdiffusion coefficients from in-depth profile measurements. This analysis was extended and modified to account for grain boundary diffusion coefficients by observing the time for "first-appearance" at a surface using the detectability limits of AES or SIMS ($\sim$0.1 atomic %).[3]

Because of the sensitivity and truly surface (e.g., Auger electrons evolve from layers 10 A or less for AES, typically) nature of the techniques, they can also be utilized to uncover process related performance-inhibiting layers (e.g., oxides at interfaces). Isotopes and oxide states can also be identified with some reasonable care.

III. THE PROBLEMS--SPECIFIC CASES

In this section, several interface and interdiffusion problems are cited. Some are examples from solar cell cases, and other are meant to be representative of a broad range of related problems.

A. InP With CdS and Schottky Barriers

InP has been demonstrated as a useful material in heterojunction and Schottky barrier devices. The single crystal, thin film CdS/InP solar cell has been reported to be stable at temperatures to 200°C in room ambient.[4] A thin film version of this device has been reported with similar stability and no detectable interdiffusion at these temperatures.[5]

The effects of heat treatments on metal-InP Schottky barriers has been reported using SIMS.[6] Au, Al, Cr, Ni, and Ti were used and SIMS distribution profiles of elemental species were obtained as a function of heat treatment to determine the progressive interdiffusion between the metal and InP. Figure 3a presents a three-dimensional composite for the Al-InP case. No degradation is noted until some P outdiffusion at 500°C. In contrast, Figure 4a shows SIMS data for a Au-InP device. The profile is well behaved to 275°C, with negligible interdiffusion. Above 350°C, In outdiffuses and at 500°C, In builds-up in the Au, forming an alloy. The accompanying effect on barrier height is tabulated with the figure. The Ni/InP and Ti/InP profiles are shown in Figures 3b and 4b respectively. A summary of the metal-InP barriers, the temperature treatment, barrier effect, and degradation mechanism is presented in Table 1. The interdiffusion and barrier degradation correlate well in each case.

B. GaAs

Similar interdiffusion effects have been reported for Ta-GaAs Schottky barriers, using AES.[7] Figure 5a presents AES data exhibiting the interdiffusion problem for both sputtered and e-beam evaporated Ta films. The corresponding barrier height degradation is shown in Figure 5b. For this system, the onset of interdiffusion can be detected at 125°C. At 450°C, the total thickness of the interdiffused layer has been measured at 1000 Å after 1 hour. Interdiffusion and barrier height effects in W(Ti)/n-GaAs diodes are shown as a function of annealing in Figure 6. AES techniques have revealed that Au has diffused through the 1000 Å W(Ti) layer to the GaAs interface, after annealing at 500-600°C for 15 hours.[8]

C. Amorphous Si

Amorphous Si films prepared by glow discharge have been shown to contain considerable amounts of bonded hydrogen (10-50 atomic %). SIMS has been used to examine the outdiffusion of hydrogen which could be disasterous to solar cells. Carlson[9] has measured the diffusion, and Figure 7a shows the profiles of the control deuterated sample and a sample heated for 25 hours at 300°C. The diffusion coefficient of deuterium is found to be[9]

$$D = 1.17 \times 10^{-2} \exp(-1.53 \pm 0.15/kT). \quad [1]$$

The diffusion coefficient for hydrogen should be slightly larger, but a 10^4 year time for film degradation due to hydrogen loss can be estimated.

D. Cuprous Oxide

Barrier heights in cuprous oxide Schottky barriers have been disappointingly lower than predicted. Recent AES work has shown that oxygen diffusion from the cuprous oxide to the metal interface (e.g., Mg) forms a metal oxide layer (e.g., MgO) and leaves a copper rich layer behind.[10] This occurs at essentially room temperature (during evaporation) and lowers the barrier height to an undesirable and unacceptable level.

E. Cu_2S/CdS

The extent of the copper diffusion problem at the junction region of this device is not yet fully identified or understood. In some materials, an irreversible degradation results and is attributed to the electrochemical decomposition of the copper sulfide and diffusion of the copper along the boundary regions.[11] In other Cu_2S material, similar or more devastating operating conditions have not shown this effect. The interdiffusion at the junction interface needs more attention, and it is expected that interpretable information can be gained from current work on more planar heterointerfaces.

F. Cu-Ternaries

$CdS/CuInSe_2$ thin film polycrystalline solar cells have been produced in both frontwall (i.e., illumination through the ternary) and backwall (i.e., illumination through the CdS) configurations.[12] In cases where the initial ternary layer is removed from the vacuum system and etched, an oxide layer results at the junction interface. The extent of the resulting oxide region can be limited but not eliminated by etching. A high series resistance results when such an oxide is present, limiting both J_{sc} and the fill-factor. The detected oxide layer is shown in Figure 8.

$CdS/CuInSe_2$, $CdS/CuInS_2$, and $CdS/CuInTe_2$ devices exhibit an interdiffusion degradation mode when the junctions are heated above 500K.[13] Diffusion of the Cd from the CdS into the ternary has been observed using AES techniques for all devices. As an example, Figure 9 shows a depth-compositional profile of a $CdS/CuInS_2$ thin-film device with $\eta = 3.2\%$, $V_{oc} = 0.51$ V and $J_{sc} = 11.8 mA/cm^2$. An orderly change from n-CdS to p-$CuInS_2$ is evident. Figure 10 shows the same device junction region after a 3.5 hour, 600K anneal. The most apparent effect of this treatment is the diffusion of Cd into the ternary film. Using the Hall-

Morabito formalism,[3] the grain boundary diffusion coefficient has been determined, and follows the relationship[13]

$$D' = D_0 \exp(-E_a/kT) \qquad [2]$$

for the data presented in Figure 11. Values of the D_0 have been determined: D_0 = 13.8 cm^2/sec ($CuInS_2$); 10.6 cm^2/sec ($CuInSe_2$); and 5.05 cm^2/sec ($CuInTe_2$). The activation energies are 1.7, 1.5, and 1.38 eV respectively. Unlike the Cu_2S/CdS device, the diffusion of Cu is not discernible over this temperature range. Device characteristics are stable for these heterostructures operating up to 423K. Definite, irreversible degradation in performance is experienced for operating temperatures in excess of 500K. These data may cause some concern for device lifetimes under severe operating temperatures.

G. SnO_x/Si

A major source of degradation for the SnO_2/Si heterojunction solar cell has been identified as a thin silicon oxide layer at the SnO_2/Si interface.[14] Figure 12 shows the major differentiated Auger spectra for Sn, O and Si at (a) the SnO_2 layer, just before the junction, (b) the junction interface, and (c) the silicon bulk, just after the interface. Both the energy position and shape of the oxygen peak change over the region. These data have been used to identify the interfacial layer as SiO_2. A calculation of the rate of oxygen diffusion to the interface predicts a rate some 12 orders of magnitude lower than observed at the processing and operation temperatures. However, the activation energy associated with the growth of the layer is 1.1 - 1.3 eV, indicating that the oxidation results from field aided diffusion of O_2 - ions. Similar degradation and diffusion effects have been noted for ITO/Si cells at elevated temperatures.[14]

IV. SUMMARY

Much work remains to be done on controlling interdiffusion mechanisms in thin polycrystalline solar cells. The minimization of such degradation processes poses a major challenge.

ACKNOWLEDGEMENTS

The author wishes to express his appreciation to Dr. S. Wagner for his suggestions and encouragement in preparing this discussion. The assistance of D. Carlson, A. Rothwarf, L. Olson, and the authors of the papers used as examples in this presentation is gratefully acknowledged and sincerely appreciated.

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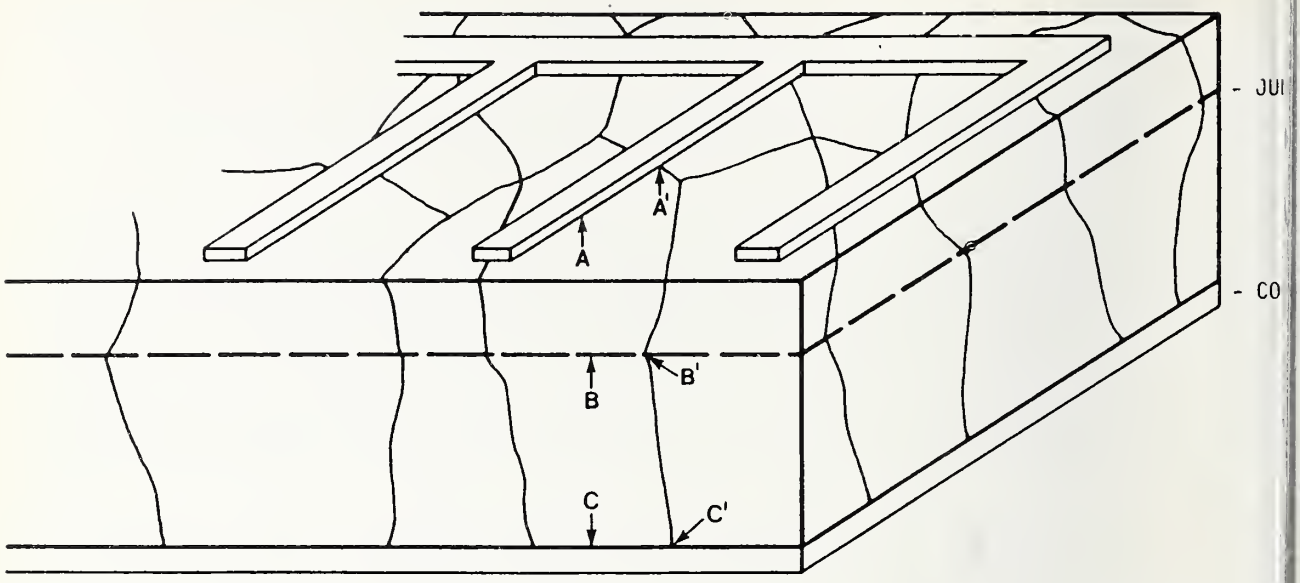


Fig. 1. Schematic representation of thin-film, polycrystalline photovoltaic device.

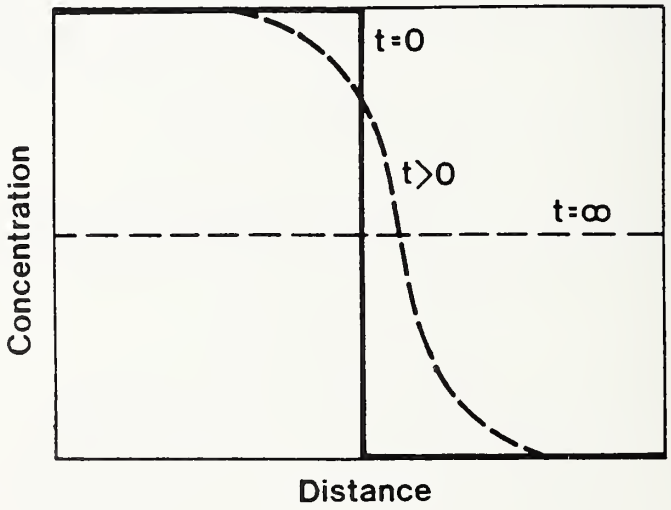
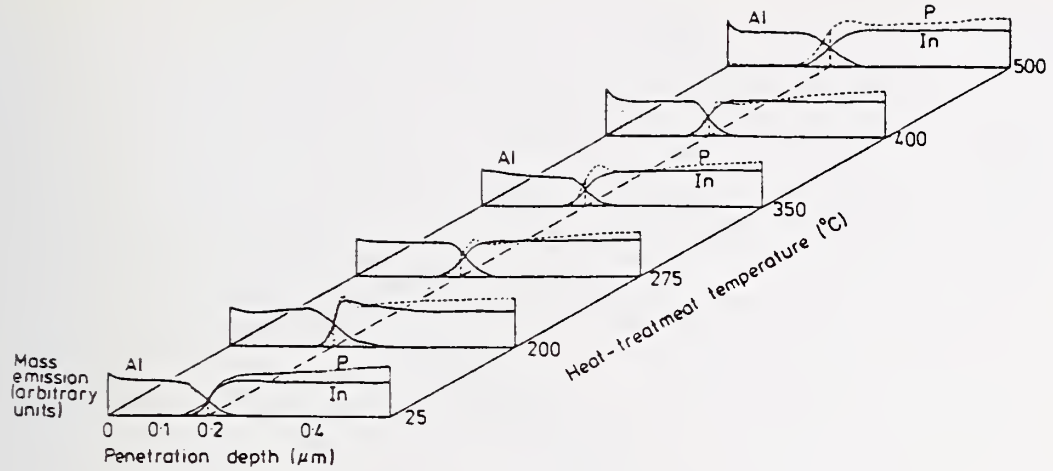
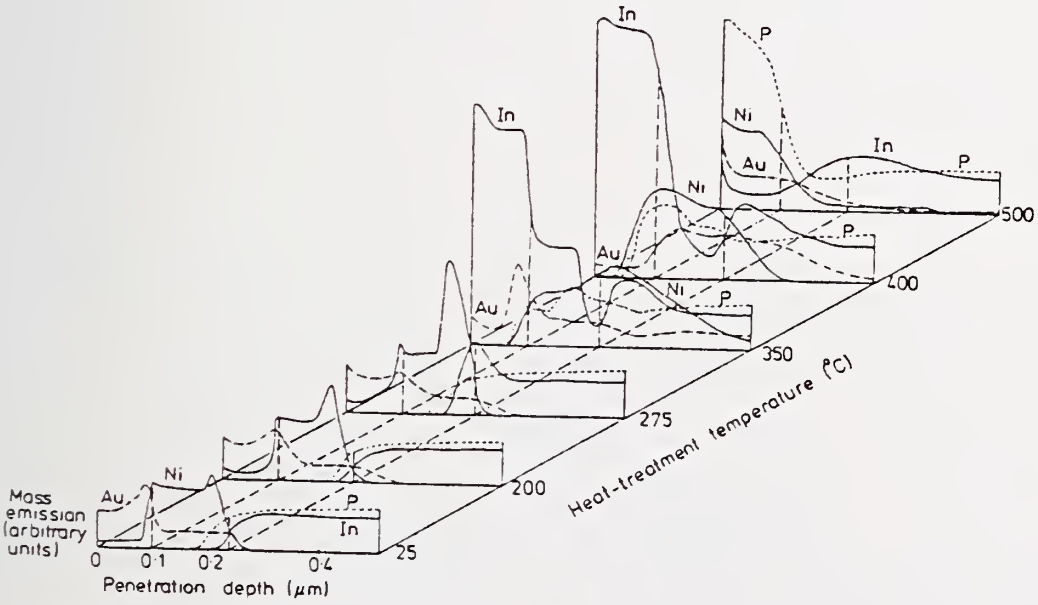


Fig. 2. Graphical representation of the interdiffusion process. "t" indicates time.



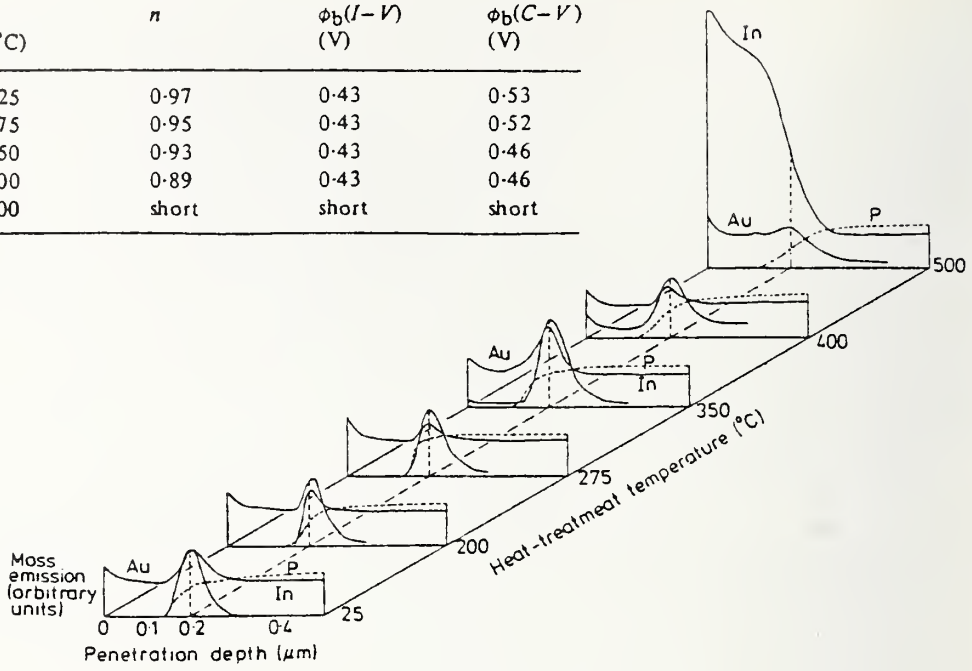
(a) Al/InP composite



(b) (Au)-Ni/InP composite

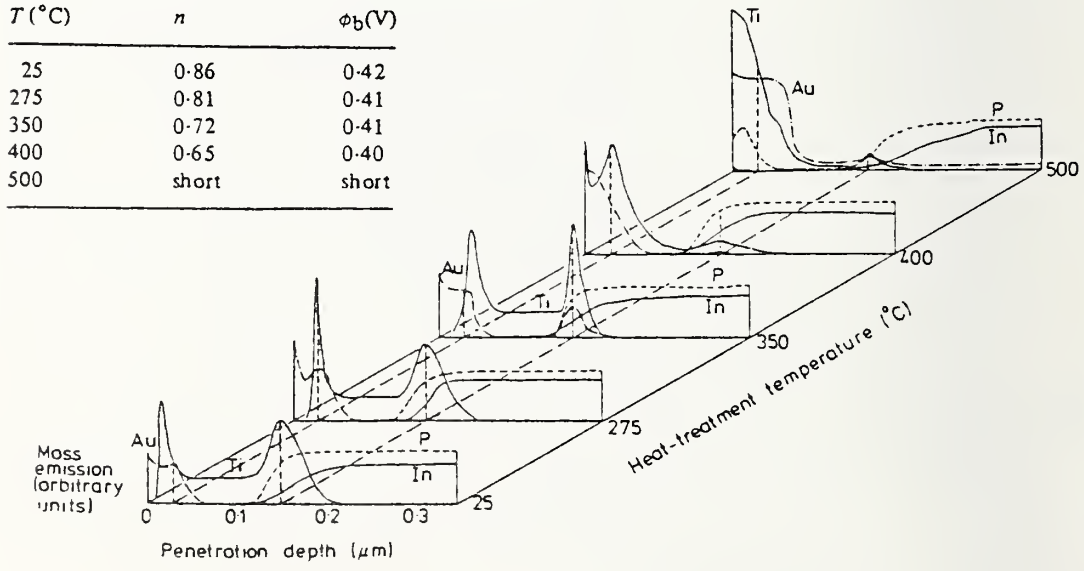
Fig 3. SIMS depth profiles for InP Schottky barrier devices. (After H.B. Kim et al., Instit. of Phys. Conf. Series, 33b, 145 (1976).

T (°C)	n	$\phi_b(I-V)$ (V)	$\phi_b(C-V)$ (V)
25	0·97	0·43	0·53
275	0·95	0·43	0·52
350	0·93	0·43	0·46
400	0·89	0·43	0·46
500	short	short	short



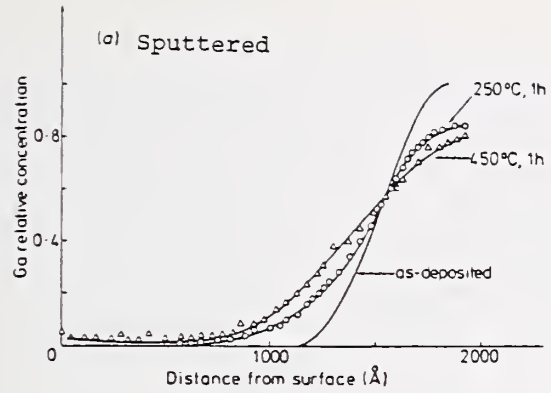
(a) Au/InP composite

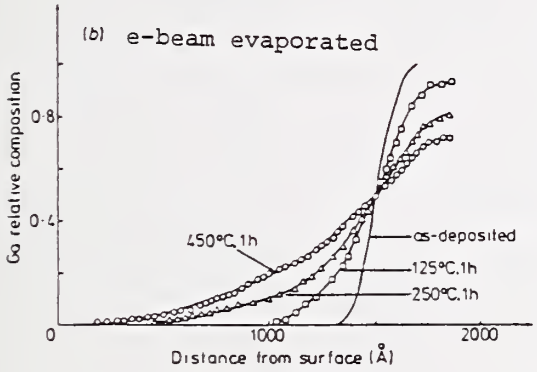
T (°C)	n	ϕ_b(V)
25	0·86	0·42
275	0·81	0·41
350	0·72	0·41
400	0·65	0·40
500	short	short



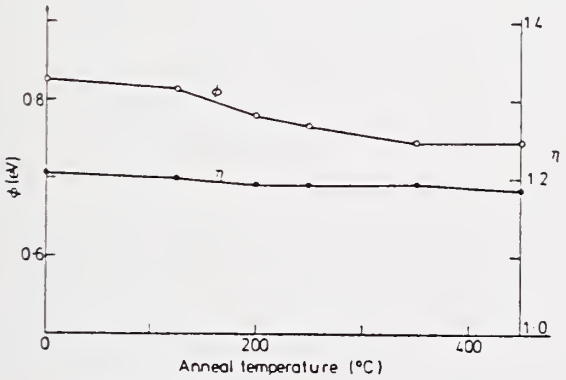
(b) (Au)-Ti/InP composite

Fig. 4. SIMS depth profiles for InP Schottky barrier devices. (After H. Kim et al., Inst. of Phys. Conf. Series, 33b, 145, (1976).



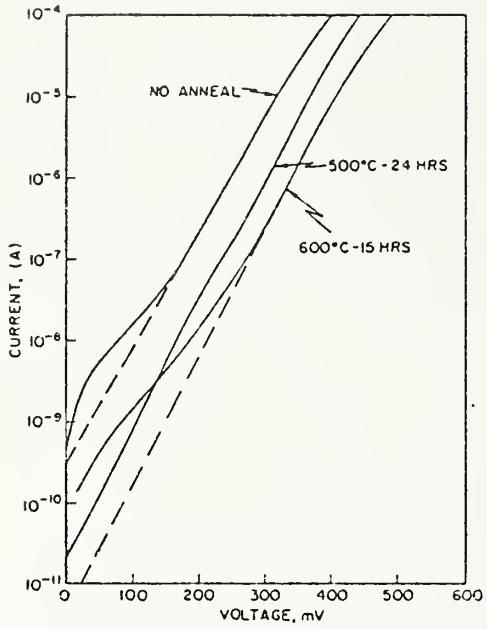


(a) AES Profiles

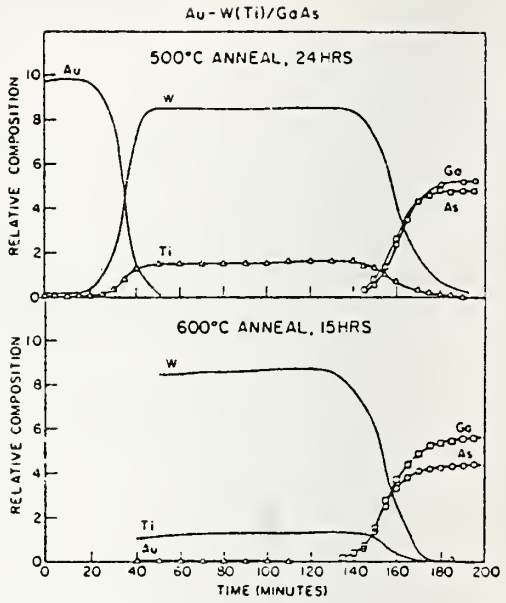


(b) Barrier heights

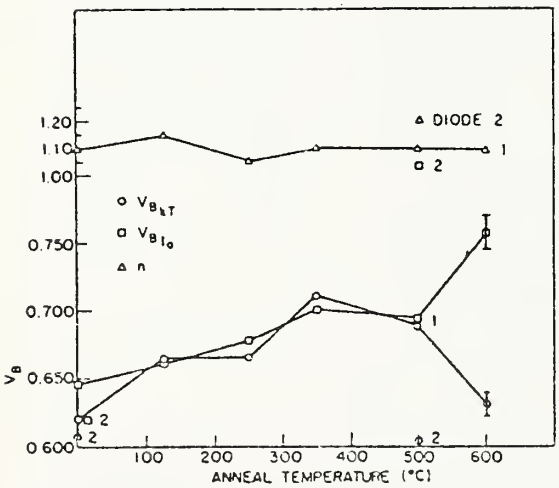
Fig. 5. AES profiles of Ta/GaAs Schottky barriers and related barrier height variations. (A. Christou and K. Sleger, Instit. of Phys. Conf. Series #33b, 1976.)



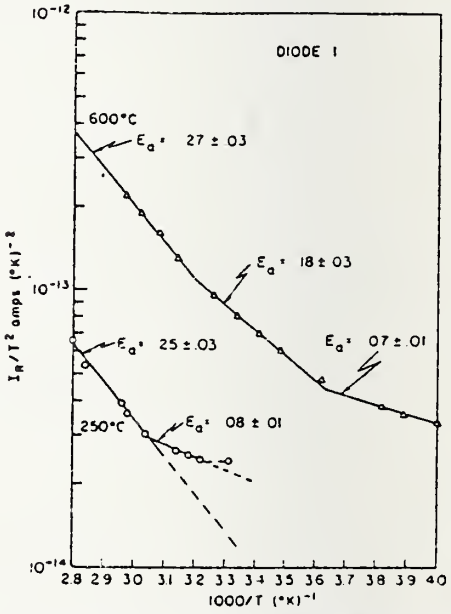
(a) I-V characteristics of Au-1000A W(Ti)/ n-GaAs Schottky barriers vs anneal temperatures.



(c) AES depth profiles of Au-1000A W(Ti) metallization on GaAs.

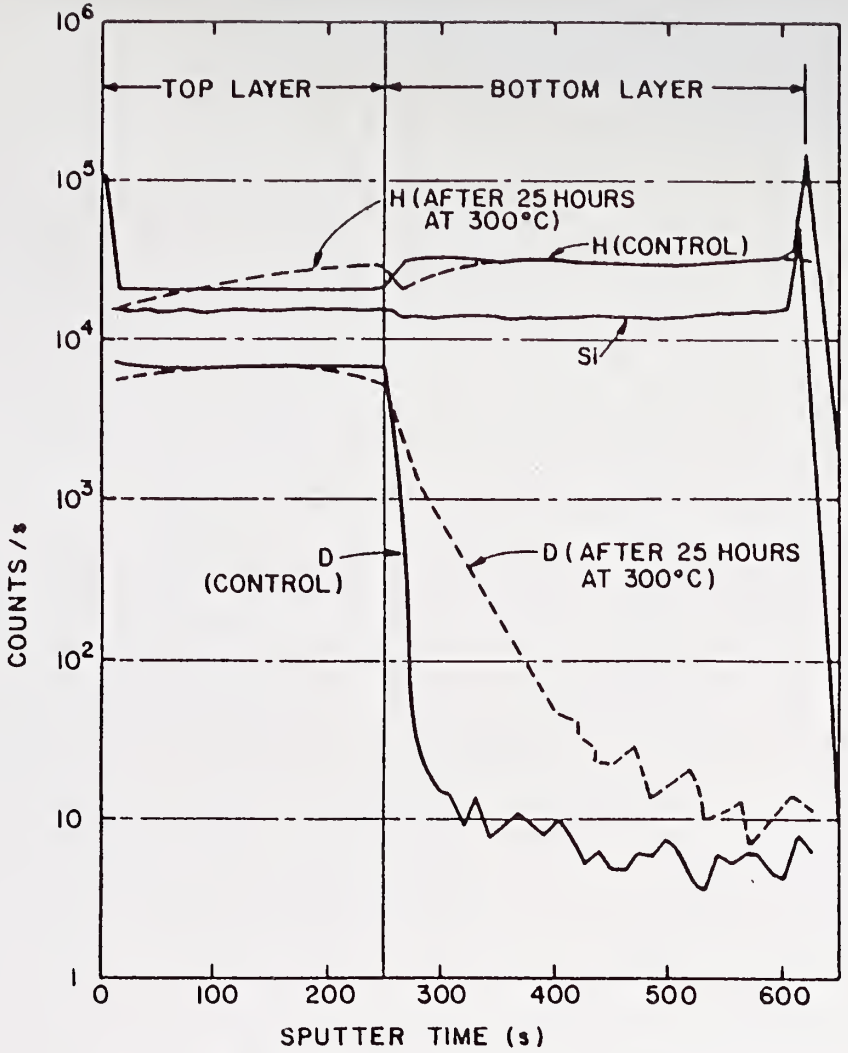


(b) Schottky barrier heights vs anneal temperature for Au-1000A W(Ti)(diode 1) and Au-100A W(Ti)(diode 2) metallizations on n-GaAs.

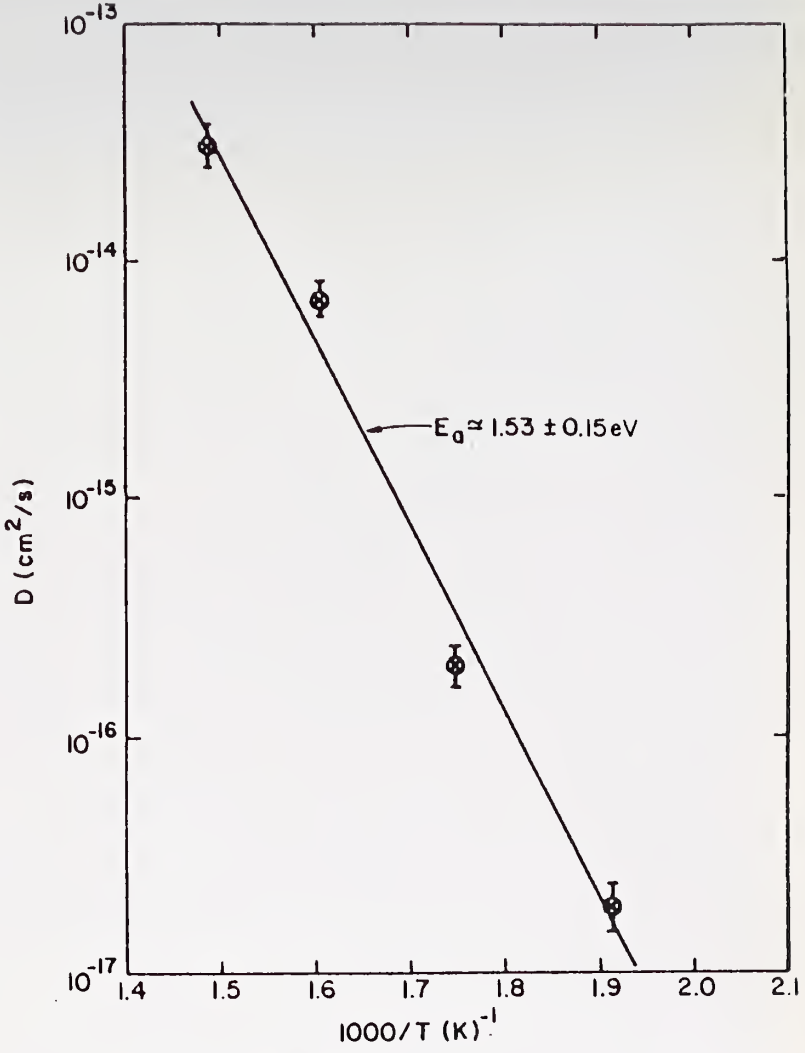


(d) Activation energy analysis of Au-1000A W(Ti)/n-GaAs diodes annealed at 250C (24 hrs) and 600C (15 hrs).

Fig. 6. Interdiffusion and Schottky-barriers in Au-W(Ti)/n-GaAs devices. (H.M.Day, A. Christou and A.C. Macpherson, J.Vac.Sci.Technol. 14, 939 (1977).



(a) SIMS profiles of a layered sample before and after 25 hrs at 300 C.



(b) Deuterium diffusion coefficient as a function of inverse temperature.

Fig. 7. Amorphous Si diffusion studies. (After Carlson, to be published in Appl. Phys. Lett.)

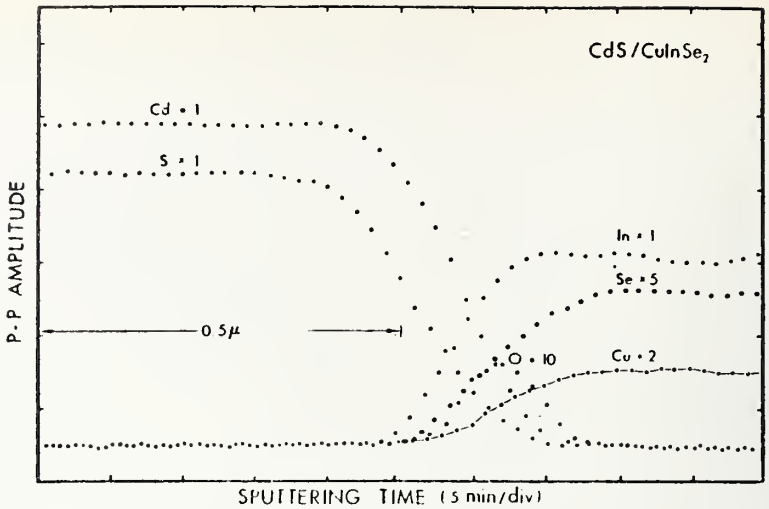


Fig. 8. AES profile of etched junction. The processing involves an external H_2Se anneal and a mild HCl etch prior to CdS deposition.

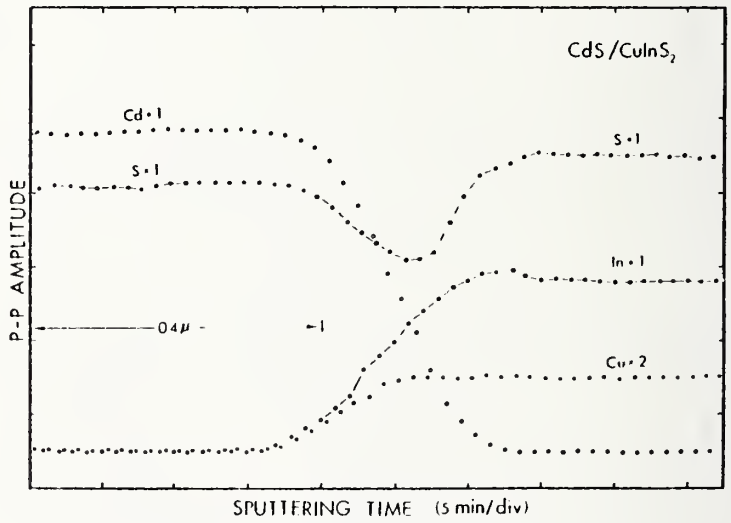


Fig. 9. AES depth compositional profile of $CdS/CuInS_2$ thin-film solar cell with 3.2% efficiency.

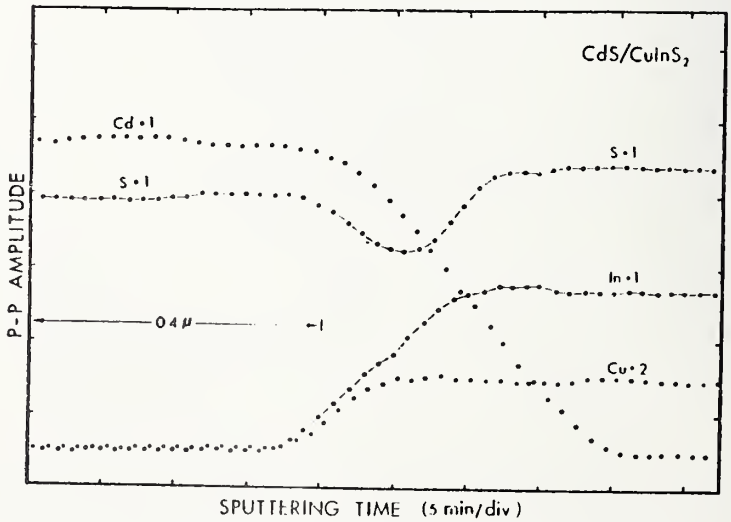


Fig. 10. AES depth compositional profile of device annealed for 3.5 hrs at 600K.

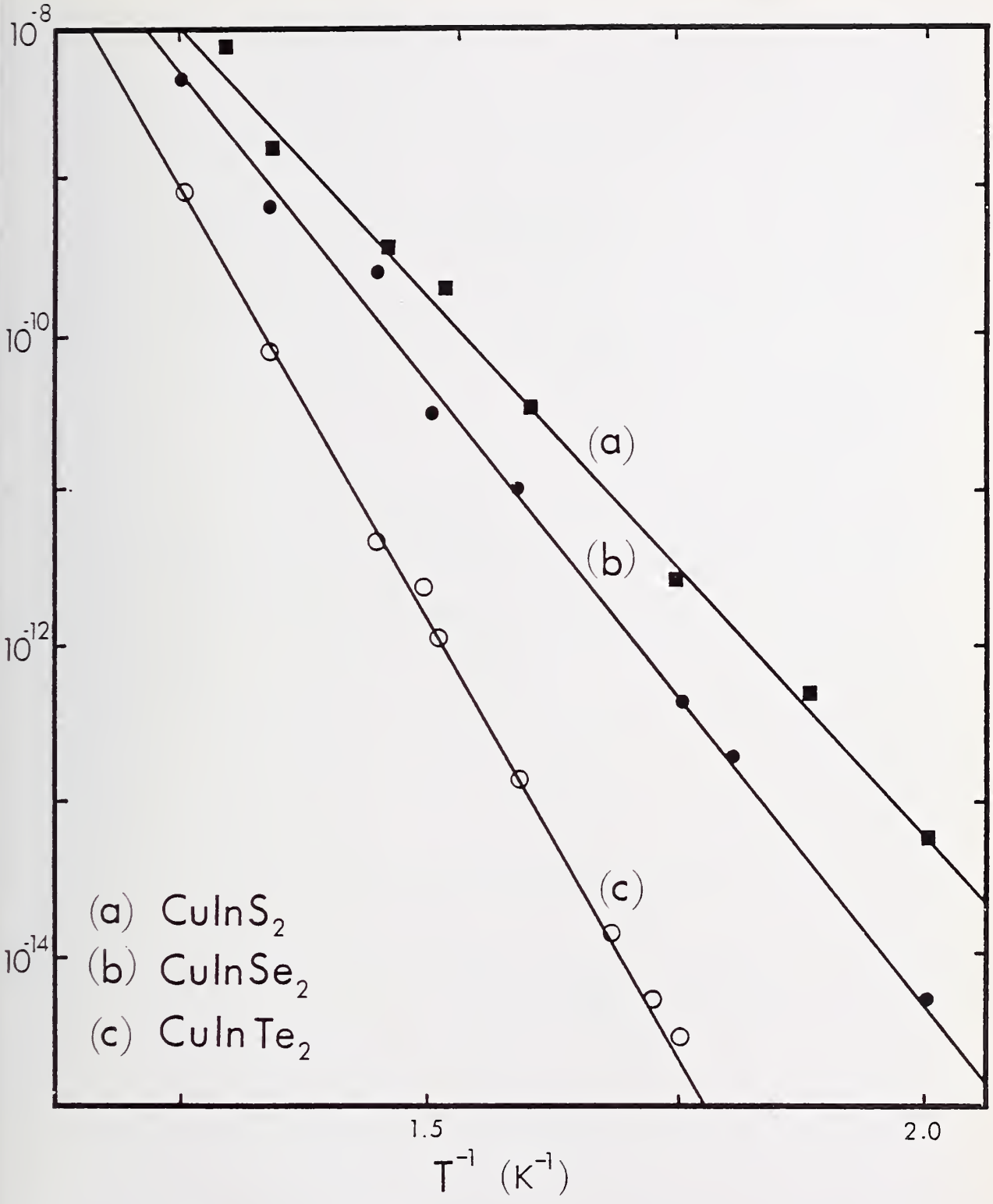


Fig. 11. Temperature dependence of grain boundary diffusion coefficient, D' for Cd from the CdS thin film layer.

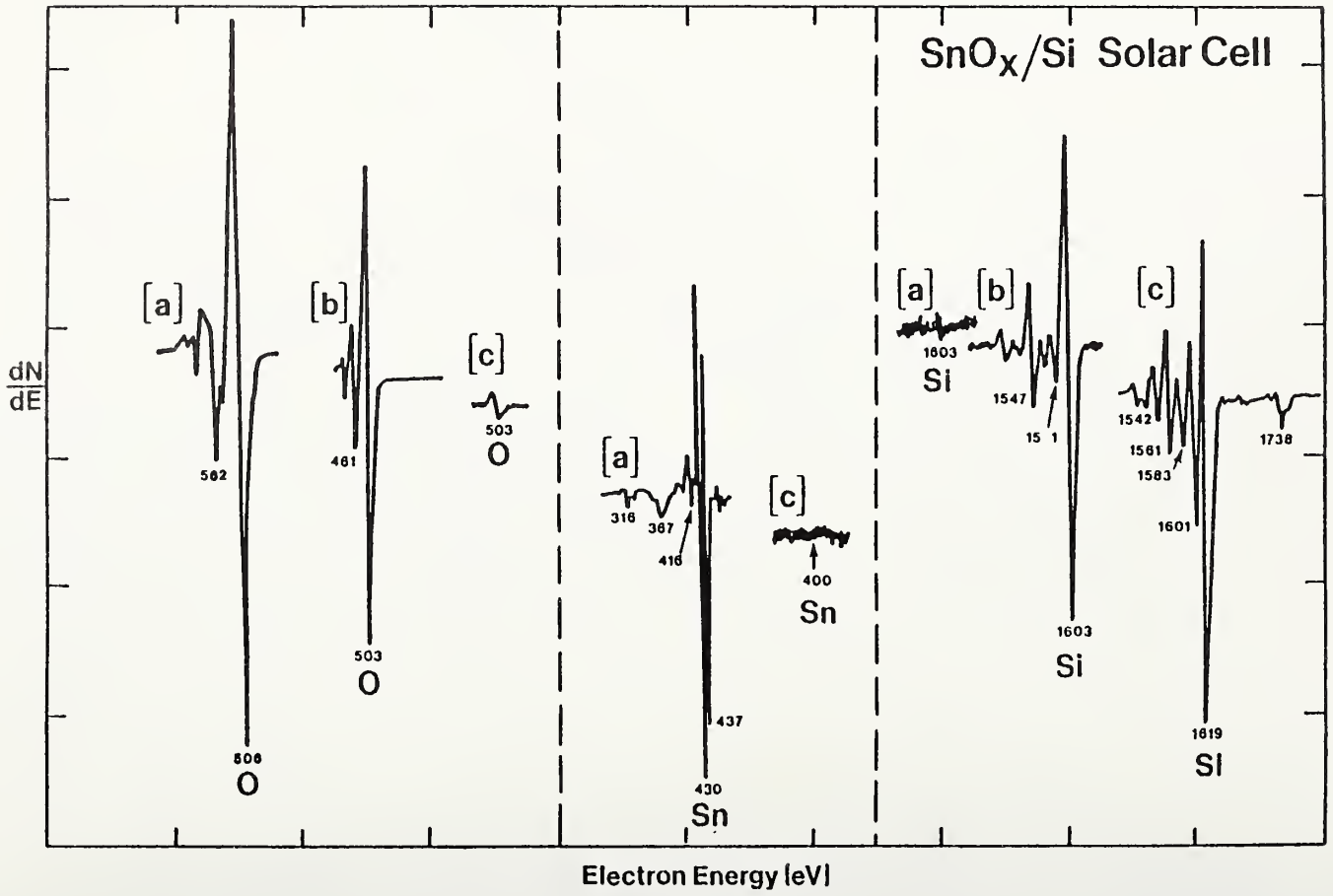


Fig. 12. Differentiated AES spectra for SnO_x/Si heterojunction solar cell. (a) is in SnO_2 layer, just before interface, (b) is detected SiO_2 layer at interface, and, (c) is in Si, just after junction interface.

Table 1. Metal - InP Schottky Barriers

Metal		T (°C)	n	$q\phi_b$ (eV)	Degradation Mechanism	Safe T(°C)
Au	Before		0.97	0.43	Au indiffusion	
	After	400	0.89	0.43	In outdiffusion	350
Al	Before		1.11	0.50		
	After	500	1.24	0.52	Stable	500
Cr	Before				Metallurgically	
	After	500	- short -		Stable	500
(Au)-Ni	Before				Catastrophic	275
	After	350	- short -		Au,Ni indiffusion In, P outdiffusion	
(Au)-Ti	Before		0.86	0.42	Au diffusion	
	After	400	0.65	0.40	P outdiffusion	350

H. M. Kim, et al., Proc. Sixth Intl. Sym. GaAs and Related Compounds, St. Louis, MO, pp. 145-153 (1977), Inst. of Phys. Conf. Series, 33b.

CORROSION AND ITS CONTROL

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The exact nature of the corrosion problems that may be encountered in any given situation depend on the device and its environment. Important considerations are the metallizations, their spacings, the voltages existing between conductors, the insulation resistance of the substrate, the quantity of adsorbed and absorbed water, cleanliness of the surface, and the composition and temperature of the environment.

Electronic circuits are primarily susceptible to electrolytic corrosion in the presence of moisture and electrical bias and to galvanic corrosion when dissimilar metals are in contact. Stress corrosion may be a problem with some electrical leads.

Electrolytic corrosion occurs when there is an electrical bias between two conductors and the resistance between them is sufficiently low so that the potential drops across the anode/insulator and cathode/insulator interfaces exceed the critical values required to initiate the anodic corrosion reaction and its cathodic counterpart. The resistance of the insulator is reduced by moisture adsorbed on its surface and by the presence of ionizable impurities. It is well known that most plastics, polymers, glasses, silica, alumina, etc. readily adsorb water from the atmosphere. Moisture can reach the surface of a device by diffusion through a cover coat or by ingress through a faulty seal. The corrosion rate is greatly increased by ionic contaminants that increase the conductivity of the adsorbed moisture layer. Failure of a device results either from the development of a high resistance as a segment of a conductor stripe is corroded, from a short circuit caused by the redeposition of the anodic dissolution product at the cathode in the form of dendrites, or from leakage between conductors caused by the spreading of the corrosion product across the device surface. Electrolytic corrosion may also occur on the external leads of devices exposed to high humidity and an electrical bias. All metals, including gold, are subject to electrolytic corrosion given the right conditions.

Many electronic components have areas of contact between dissimilar metals, which in the presence of moisture may lead to galvanic corrosion. This is especially true if a noble metal, such as gold or copper, is in contact with an active metal, such as aluminum.

Stress corrosion is a sporadic problem in the electronics industry and is frequently guarded against by electroplating the susceptible alloy. An example of such a material is a proprietary iron-cobalt-nickel alloy often used as lead wire in devices requiring metal-to-glass seals. When properly coated, e.g., gold plated, the lead will not crack. However, if the coating is not continuous, as may happen at points of stress or mechanical damage, the alloy will crack in the presence of chlorides and moisture and sufficient applied or residual stress.

Many corrosion problems can be avoided by proper design and choice of materials and by rigorous efforts to avoid contamination of the device. The design should maximize insulation resistance, avoid contact of dissimilar metals at sites susceptible to the ingress of moisture, and choose cover coats or packages that prevent the migration of moisture or other contaminants to the device surface. Contamination must also be avoided during the manufacturing process. For example, residual plating salts must be completely washed away, and activated fluxes should not be used.

Solar cells will, of course, be exposed to the atmosphere and, therefore, to dust. Many instances of corrosion can be attributed to dust particles. These may be (1) intrinsically corrosive, absorbing moisture from the atmosphere to form an electrolytic solution, or (2) indirectly corrosive, absorbing both moisture and corrosive agents from the atmosphere or being conductive and serving as a cathode, or (3) essentially harmless, but on occasion producing a geometry conductive to crevice corrosion.

TERRESTRIAL SILICON ARRAY FIELD AND TEST EXPERIENCE*

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The key building block of a photovoltaic system utilizing flat plate silicon solar arrays is the solar cell module. The solar cell module consists of a collection of solar cells electrically interconnected in series/parallel and encapsulated into a mechanical package which provides for structural support and protection from the terrestrial environment. In the system, the modules are interconnected to form solar arrays consistant with the current and voltage requirements of the particular application.

The design of solar cell modules, like any design, is based on providing an optimum compromise between the competing demands of improved system integration, higher reliability/lifetime, and lower manufacturing cost. A key consideration in the design of solar cell modules is the identification and resolution of the life-limiting or safety-related failure modes and mechanisms.

The most important information on failure modes of silicon flat-plate solar cell modules has come from field experience. As indicated in the subsequent viewgraphs there are six key failure modes currently encountered with flat plate silicon modules.

- Electrical Interconnect Breakage
- Solar Cell Cracking
- Encapsulant Cracking & Delamination
- Cell Metalization Deterioration
- Electrical Insulation Breakdown
- Optical Surface Soiling

These failure modes are listed in approximate order of severity in early modules of the pre-1976 time period. In recent years electrical

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interconnect breakage, metalization deterioration, and electrical insulation breakdown have been substantially solved. Considerable progress has also been made in the remaining areas. It is probably safe to assume that these same failure modes will be important in thin film arrays.

The approach used to solve the early module design weaknesses is based on identifying the failure mechanisms and engineering a design solution. A difficult aspect is assessing the adequacy of the solution or comparing the relative strengths of alternate solutions in a short time period. This has been addressed through the use of qualification tests designed to environmentally stress the modules and precipitate failures expected in field use. Selection of the test environments is a difficult task based on engineering judgement and extensive test experimentation. Correlation with the actual field environment, where it exists is based primarily on historical (empirical) evidence. Direct correlation is rarely achieved due to the unknown nature of the actual field environment and the generally unknown sensitivity of the failure mechanism to the accelerated test environment.

Those environmental tests found to be most useful in module design qualification, or screening are described in the viewgraphs. Of these the thermal cycle, humidity and structural tests have proved to be excellent. Ultraviolet testing has been found to be difficult to interpret and unreliable to date. Research on ultraviolet-humidity, bias-humidity, and module soiling tests is actively being pursued within the silicon program. Additional tests are examined for use when field failure mechanisms are identified which are not precipitated by the current environmental tests.

LOW-COST SOLAR ARRAY PROJECT

KEY FAILURE MODES AND MECHANISMS

- ELECTRICAL INTERCONNECT BREAKAGE
  - THERMAL CYCLING
  - WIND LOADING
- SOLAR CELL CRACKING
  - THERMAL CYCLING
  - HAIL IMPACT
- ENCAPSULANT DELAMINATION AND CRACKING
  - THERMAL CYCLING
  - HUMIDITY
  - ULTRAVIOLET
- CELL METALLIZATION DETERIORATION
  - HUMIDITY (BIAS-HUMIDITY)
- ELECTRICAL INSULATION BREAKDOWN
- OPTICAL SURFACE SOILING

LOW-COST SOLAR ARRAY PROJECT

ENVIRONMENTAL QUALIFICATION TESTING

- OBJECTIVE:
  - UNCOVER POTENTIAL FIELD FAILURE MODES AND MECHANISMS TO ALLOW FOR THEIR ASSESSMENT AND CORRECTION
- APPROACH:
  - SUBJECT MODULES TO CAREFULLY CHOSEN EXTREME ENVIRONMENTS WITH KNOWN IMPORTANCE
- PHILOSOPHY:
  - MINIMUM TEST COMPLEXITY TO REDUCE COST
  - MAXIMUM TEST STABILITY TO ALLOW CORRELATION AND COMPARISON

LOW-COST SOLAR ARRAY PROJECT
KEY ENVIRONMENTAL TESTS

- CURRENT PRACTICE
  - THERMAL CYCLING: -40 TO +90°C, 50 CYCLES
  - HUMIDITY: MIL STD 810°C, 507.1, V
  - MECHANICAL CYCLING: ±50 lb/ft^2, 10,000 CYCLES
  - TWISTED MOUNTING SURFACE: 1/4 in/ft
  - HAIL IMPACT: ICE BALL PROJECTILES
  - VOLTAGE BREAKDOWN: 1500 VOLT HI-POT
- UNDER DEVELOPMENT
  - OPTICAL SURFACE SOILING
  - BIAS-HUMIDITY
  - UV-HUMIDITY

LOW-COST SOLAR ARRAY PROJECT
OTHER TESTS

- SPECIAL ENVIRONMENTS
  - SALT FOG
  - FUNGUS
- TESTS HAVING LITTLE EFFECT
  - HUMIDITY-FREEZING
  - HEAT-RAIN
  - WIND DRIVEN RAIN
  - WEATHEROMETER
  - SHIPPING SHOCK AND VIBRATION
  - DUST ABRASION

METHODOLOGY FOR DESIGNING ACCELERATED AGING TESTS FOR PREDICTING LIFE OF PHOTOVOLTAIC ARRAYS

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A life of 20 years in terrestrial environments, a goal for photovoltaic systems, is a new requirement for electronic devices. In order to justify large expenditures for large-scale solar installations it must be established, by appropriate testing, that candidate photovoltaic systems have the potential for surviving terrestrial environments for a minimum of 20 years. It is clearly not acceptable to conduct a 20 year test at a specific terrestrial site simply to determine whether the device will last 20 years at that site. Instead of subjecting candidate devices to the normal stresses associated with a terrestrial site, it is generally considered necessary to subject the devices to laboratory tests involving higher-than-normal stresses. The general objective of such accelerated testing is to cause the devices to age more rapidly than under normal-stress conditions, subject to the constraint that the devices degrade for the same reasons as would have occurred under normal stress conditions. The phrase "to degrade for the same reasons" is intended to mean that exactly those rate processes associated with degradations in performance and structure in the normal environment are activated by the test conditions involving the higher-than-normal stress environments. Ideally, the over-stress conditions uniformly accelerate the normal rate processes so that 20 years of aging may be identified in a relatively short time period, say two years. Such idealized considerations have led to the concept of an acceleration factor in which, for example, an acceleration factor of 10 is said to exist whenever one hour of laboratory testing is equivalent to 10 hours of field exposure.

There are a number of well-known hazards associated with accelerated laboratory tests conducted at higher-than-normal stress levels. The primary threat to the validity of accelerated testing lies in the fact that operation of the devices at higher-than-normal stresses may cause the devices to fail for the wrong reasons; that is, the over-stress conditions may activate degradation modes that may never occur under normal-stress conditions. An additional hazard is related to the fact that extrapolation, not interpolation, is required in order to predict the duration of life under normal-stress conditions by means of data obtained under higher-than-normal stress conditons. Moreover, normal stress conditions are not well-defined simply because the normal environment at Miami, Florida is quite different from that at Bismarck, North Dakota. This greatly complicates the problem of determining which variables should be controlled in the laboratory setting. Even mundane problems of what constitutes unacceptable degradations in performance, definitions of end-of-life, etc., cannot be avoided in making valid predictions of life.

Such considerations indicate that the problem of designing accelerated aging tests is difficult. The purpose of this review is to highlight some recently proposed concepts related to a methodology for designing accelerated tests. Recent hypothetical examples have been given only for silicon solar cells. However, the basic concepts and the underlying methodology are believed to be equally valid for the accelerated testing of thin-film devices.

Historical Approaches

The literature shows a variety of approaches to the basic problem of accelerated testing. Some authors have treated accelerated testing as problem of estimating the parameters in a mathematical model. In such an approach, the behavior of the primary degradation mechanism, as a function of time and stress level, is assumed to follow a known mathematical model. The models associated with Arrhenius, Eyring, and the power law in References (1) through (5) are examples of this approach. The primary objective of this approach is to obtain valid numerical estimates of the model parameters using data taken under over-stress conditions.

When the model is not assumed to be known, then the data itself must be used to identify and extract candidate models. This data-analysis approach to accelerated testing is exemplified in References (6) through (8). The resulting quantitative relationships may be characterized as physical (based on accepted quantitative models related to the physical degradation processes), statistical (based on linear or non-linear polynomial regressions assumed to approximate the unknown physical relationships) or empirical (based on simple correlations that are found to be significant and persistant over time). The risks associated with extrapolation from over-stress to normal-stress conditions emphasize the desirability of using models based on the physics of the dominant degradation mechanisms. Statistical models, and especially empirical models, are usually avoided whenever possible. However, it must be recognized that the actual behavior of a device, subjected to simultaneous exposure to a combination of different stresses (temperature, moisture, UV radiation, etc.) is often first expressible in terms of simple correlations, subsequently expressed in terms of statistical relationships, and finally expressed in terms of physical mechanisms.

The methodology summarized below explicitly recognizes that accelerated testing can also be regarded as a problem of experimental design, see References (9) through (15), and as a problem of extrapolation, see References (16) through (19). The methodology was developed for the Low-Cost Silicon Solar Array project directed by ERDA/JPL. More complete details are presented in Reference (20).

Idealized Accelerated Tests

An idealized accelerated test consists of operating a number of nominally identical solar devices at a higher-than-normal stress S_1; operating a second set of devices at a still higher stress S_2; etc. At least 5 stress levels, S_1, . . . , S_5, are used with a minimum of 5 devices tested at each stress level. Performance over time is monitored by making periodic measurements. In the simplest case linear degradations are obtained over time, with the largest time rate of degradation associated with the highest stress. In some cases, a plot of the logarithm of the degradation rate versus reciprocal stress (an Arrhenius-type plot) yields a straight line. The straight line serves as limited evidence that the degradation mechanism has not changed over the range of over-stress test conditions used in the experiment. At some risk it may then be assumed that the same degradation mechanism holds at the extrapolated normal-stress conditions S_0. The Arrhenius plot is then extrapolated to obtain an estimate of the degradation rate under normal stress conditions. The magnitude of the extrapolated degradation rate under normal stress is then used as a basis to predict the life of the device. Although greatly oversimplified, this idealized approach has served as a basis for a wide variety of accelerated testing in the electronics industry. Even where the approach proves to be too simple, the data obtained from such testing often yields an improved and useful understanding of the aging behavior of the device under various stress conditions.

Additional Requirements

A terrestrial environment involves more variables and more stress conditions than can be included in a laboratory test program. Highly sophisticated instrumentation is required in order to detect and measure very small degradations at the earliest possible time. Changes in calibration, drifts in the "controlled" stress levels, power failures, and miscellaneous accidents that occur over a two year time period often threaten the validity of accelerated test data.

Such considerations underscore the importance of performing accelerated tests only on solar devices that have mature designs and are produced by well-controlled fabrication processes having extremely high standards of uniformity and quality. A full-scale accelerated test is an expensive way to discover that the test devices suffer from infant mortality, are not uniform, or require essential changes in design or constructions.

These arguments suggest that a unique accelerated test is likely to be required for each specific device. For such a device all materials, interfaces, junctions, etc. must be fully characterized in order to identify the possible failure mechanisms. In addition, considerable initial data should be taken using over-stress conditions to identify

and correct weaknesses in early designs or constructions. Initial performance data using over-stress conditions are also required to assure that the devices show no obvious signs of potential early degradations. Data related to abusive terrestrial stresses, such as humidity-freezing tests, salt-fog tests, rain tests, and fungus tests are important to assess the robustness of the devices. If available, data from qualification tests and acceptance tests are also useful. All such data are required to fully identify the potential failure modes and possible activating stresses to be considered in the design of the accelerated test.

To a large extent these requirements are based on common sense. Common sense also appears to require that accelerated tests be designed using the best available concepts derived from statistically designed experiments. However, in the experience of the authors, statistically designed experiments seem to be most useful when very little is known concerning the anticipated behavior of the device to be tested. The greater the prior knowledge, the more difficult it is to incorporate such knowledge into a standard statistically designed experiment. This is frequently the case when the underlying physical rate laws for some, but not all, mechanisms are known; when the performance of the device has been studied extensively under some conditions, but has been studied very little under other conditions; when some stresses are known to be of negligible importance under some operating conditions but not others, etc. All such prior information is frequently difficult, if not impossible, to incorporate into a statistically designed experiment which generally requires "balance" and orthogonality, and is conventionally analyzed in terms of polynomial regression.

The primary reason for using a statistically designed experiment is to reduce the number of test conditions (combinations of stresses) to an absolute minimum and still preserve the ability to effectively analyze the over-stress data and predict expected life under normal stress.

A Proposed Methodology

The procedure described below aims to obtain an acceptable compromise between engineering and statistical criteria for the design of an accelerated test. The primary steps of the procedure are briefly outlined as follows:

- A complete factorial table is constructed that shows all combinations of high and low stress levels for each stress under consideration. For each stress the high stress level should be chosen as high as possible under the constraint that the dominant failure modes are expected to be identical to those experienced under normal stresses. The low stress level should be chosen to yield measurable degradations within the time constraints of the accelerated test, say within two years.

- Quantitative engineering assessments are made to express the relative anticipated severity of each combination of stress levels given in the factorial layout. These prior judgments are to be made by engineers and are intended to be based on all relevant engineering knowledge.

- The numerical severity ratings for each combination of stress levels are then analyzed using a standard statistical procedure. The analysis serves to reveal the underlying implicit judgments concerning the anticipated relative importance of each stress considered individually (main effects) and the anticipated relative importance of possible synergisms (interactions) among combinations of different stresses.

- The resulting quantitative measures of the anticipated main effects and interactions are represented in graphical form as a hierarchical tree. The relationships exhibited by the tree are then reexamined for consistency with the earlier expressions of engineering judgment. Inconsistencies are removed, if necessary, by iterating the procedure several times in order to assure that engineering judgment yields the same anticipated relationships irrespective of whether the effects of the stresses of interest are considered one-at-a-time or in combinations.

- The graphical structure of the tree then permits easy identification of which combinations of stresses are most important and which may possibly be eliminated. The elimination of all but the essential test combinations of stresses reduces the number of tests (stress combinations) required for inclusion in the accelerated test program. This reduced experimental design is called the engineering design. The elimination of certain test conditions always degrades the statistical design so that only conditional main effects and conditional interactions can be obtained from the data. Although these conditions are the most appropriate conditions from an engineering point of view, the extensive confounding (ambiguous identification of the effects of the various stresses) frequently threatens the statistical validity of the engineering design.

- A mathematical technique based on Lagrange polynomials is used to obtain an exact characterization of the extent and type of the statistical confounding that exists in the engineering design. The details of this mathematical technique are to be published elsewhere (21).

- Once the statistical deficiencies of the engineering design are fully identified, it is then possible to consider adding a limited number of tests to the design in order to improve statistical validity. As each test is added, the cost of adding the test can be compared with the statistical benefits. A wide variety of fractional factorial experimental designs can be compared against the engineering design to minimize the number of tests to be added to the engineering design to achieve statistical acceptability; see References (9) through (15).

Once the general form of the design has been obtained, using 2 stress levels for each stress, the design may be expanded to include more than two stress levels for selected stresses. In general, several iterations are expected in the evolution of the design. Parametric trade-off studies, involving the number of tests and the corresponding statistical information obtained on main effects and interactions, are useful for comparing alternative designs.

- When the lowest stress level is coded as -1, and the highest stress level is coded as +1, it follows that the normal stress level will correspond to a negative number less than -1. It is necessary to scale the test range of each stress to correspond to the interval (-1,1). Historical data at terrestrial sites of interest may serve as a guide for determining the scale values corresponding to the normal level of each stress (20). The unavoidable scaling of the range of each stress constitutes one of the important steps in this experimental design procedure. Decisions made concerning the use of linear, logarithmic, or reciprocal scales, for example, have a marked effect on the "spacing" of stress levels, extrapolation procedures, etc.

- An extrapolation from the stress range (-1,1) to the normal stress level, located at -K, is increasingly hazardous for increasing values of K. To obtain maximum precision for estimated degradation rates under normal stress conditions, it is desirable to use an optimal allocation of test devices among the stress levels to be used in the accelerated test. The extrapolation procedure of Hoel and Levine (16) is used for this purpose. The number of devices required for the accelerated tests is obtained from the optimal allocation results, combined with the idealized requirement that at least 5 devices should be tested at each combination of stress levels and at least 5 stress levels should be used for each type of stress.

- The sequence of measurements over time and the associated instrumentation are based on the need to detect and measure small degradations as soon as such degradations occur.

- The data obtained from the accelerated test should be analyzed concurrently with the test program. Simultaneous efforts to analyze the data should be carried out using: (1) physical models associated with the identified degradation processes; (2) statistical regression models assumed to approximate the underlying physics; and (3) empirical models based on simple correlations. During the test program predictions should be made of the expected degradations both within and between stress conditions. This is done in order to generate a "track record" for predicting the kind and amount of degradation to be expected at later times at lower stress levels using currently available data obtained at the higher stress levels.

Conclusions

The design of accelerated tests involves striking a balance among a variety of conflicting criteria. The tests performed at higher-than-normal stress levels must provide a basis for extrapolation to normal stress levels. Of necessity, the extropolation involves an element of risk. The risk may be reduced, but not eliminated, by using several stress levels say 5, for each kind of stress. This provides a base from which the extrapolation can be carried out. It also provides a means for checking whether or not the dominant failure modes change over the range of stresses used in the accelerated test. Performing tests at stress conditions only slightly higer-than-normal reduces the extrapolation risk, but may result in no measurable degradations over a test period of two years. In such a case the acceleration factor is too small to be useful. At the opposite extreme the use of severe overstress testing results in rapid degradation but for reasons not encountered under normal stress conditions.

At the present time there seems to be no accepted criterion for indicating when a device has "matured" sufficiently to warrant being subjected to an accelerated life test. It is clear that a wide variety of initial data is needed to properly design an accelerated test: performance data, robustness data, data related to fabrication, uniformity, quality, etc. As described by the above methodology, such data forms the basis for the engineering judgments used to obtain the initial engineering design of the accelerated test. The proposed methodology then provides for subsequent iterative improvements by applying statistical criteria, and by allocating devices optimally to maximize the precision of the extrapolated degradation rates. In this way, the methodology yields a defensible compromise for the final design of the accelerated test.

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View Graph 1

DEGRADATION MECHANISMS

DIFFUSION	(MASS TRANSFER)
CHEMICAL	(CHEM. CHANGE)
ELECTROLYTIC	(ION MOBILITY)
PHOTOCHEMICAL	(PHOTON INDUCED)
MECHANICAL	(STRUCTURAL)

View Graph 2

ACCELERATED TESTING

GOAL

Project Deployment Lifetime

RULES

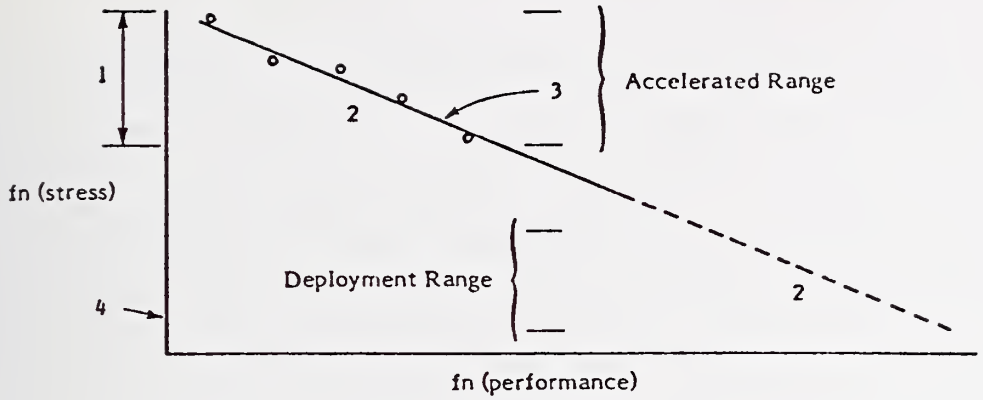
1 Establish base population

2 Establish that accelerated failure mode matches deployment failure mode

3 Establish functional relation between stress and performance.
(Note any anomalies and continuity or discontinuity of failure mechanism)

4 Conduct testing over at least 3 or preferably 5 stress levels.

View Graph 3
ACCELERATED TESTS



1 As wide as possible
2 Same failure mode
3 Continuity
4 Zero time cell population
? Synergism

View Graph 4
DEPLOYMENT-REAL TIME TESTING

INSOLATION	TOTAL PEAK SPECTRAL
THERMAL	AMBIENT DEVICE
STRESS	RESIDUAL DEPLOYMENT
ELECTRICAL LOADING	STATIC DYNAMIC
AMBIENT	HUMIDITY RAIN,DUST
ZERO TIME	SAMPLE SIZE SELECTION BASE PROPERTIES

6. Session III: Discussion Group Sessions to Identify Tests and Measurement Procedures That Can Be Used to Enhance the Prediction of Material and Device Stability

Discussion Group I on Cu_2S/[CdZn]S, Cu-Ternaries/Cds, InP/CdS, and Amorphous Si

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Group 1 covered the conventional CdS/Cu_2S cell, InP/CdS and copper ternaries with CdS. Amorphous silicon was also included in the group but, unfortunately, was virtually unrepresented for much of the discussion. I will not attempt to cover things in the order in which they were considered as the discussions tended to move from topic to topic in a somewhat random manner. The makeup of the group rather obviously influenced the areas which were of concern and on which most time was spent. Probably a majority of the group is engaged in research on what were christened "infant cells." These are cells which are so young that much of the present work is concerned more with materials than complete devices. The second major component of the group were those engaged in either research or development of the traditional CdS/Cu_2S cell. For obvious practical reasons, at least some of these people are now becoming directly concerned with cell lifetimes and stability. We were fortunate to have present representatives of both the commercial companies now entering the manufacturing stage. I will now deal with the specific topics that were discussed to a reasonable extent and in which a fair amount of consensus was achieved.

Degradation Mechanisms

The first viewgraph shows a listing of five degradation mechanisms which seem to cover all the failures that one could expect in the cells under discussion. Inter-diffusion implies mass transfer. This could be the motion of an atomic species from one part of the junction to another or in the case of amorphous silicon, this could be actual effusion of hydrogen out of the device. Under the chemical category would be things like oxidation, corrosion, or any other change in chemical state. Electrolytic decomposition implies the motion of charged ions under the influence of an electric field. Such an effect has been extensively reported for the Cu_2S component of the CdS/Cu_2S cell. Photochemical degradation would encompass any change that is directly photon induced. The final category, mechanical or structural degradation, is something of a catch-all. Typical examples would be grids lifting from the surface of the cell or delamination of various cell layers.

I think it is fair to say that much of the thinking that went into the above list was in the framework of completed devices. However, one can probably take all that was said and mutatis mutandis apply it to component materials rather than total devices. Much of the research work on infant cells will in fact involve exploring the above types of effects with regard to the component materials. In due course the studies will have to be extended to complete devices. There are, of course, a very large

number of tests and analytical procedures that will be used in exploring or investigating these degradation mechanisms, but there seems little to be gained by trying to list them.

The next subject I will cover was probably dealt with towards the end of the discussion rather than at the logical time which would have been right at the beginning. How does one define degradation? In the context of actual use of cells and deployment there was universal agreement that efficiency is the key parameter. Degradation is then the change of efficiency, presumably a reduction, over a time period. For research purposes, all the cell parameters are critical and the major concern here was that reporting of experimentation should be very full and complete. Even if the major point of an experiment is to monitor a single cell parameter such as short circuit current, the reporting should be as complete as possible and give information on all other critical aspects of the tests. A particular concern expressed was that the zero time data should be very fully given. In the absence of a complete description of cell structure and properties before degradation is induced, it is difficult if not impossible to assess the significance of the degradation data.

Accelerated Testing

Much of the discussion in this area was motivated by the paper presented by Dr. Thomas of Battelle. The second viewgraph shows the goal of accelerated testing and some rules which were suggested. The goal is to project the usable deployment lifetime from short term testing. The rules are probably not all those necessary to insure meaningful and reliable accelerated testing but represent our first efforts to provide guidance. The first requirement is to establish a meaningful base population of cells. This is what we have been calling the zero time data. It is then necessary to establish that failures induced by the stressing have their equivalence in deployment failures. In order to be able to project performance, it is necessary to establish either empirically or theoretically the functional relationship between the stressing and lifetime. In this area, questions of continuous (e.g. diffusion) and discontinuous (e.g. cracking) failure modes must be addressed. Finally, although Dr. Thomas indicated that he felt from a statistical point of view five stress levels were necessary, the experimentalists were unenthusiastic about the amount of testing that this implies. In the end we went on record as recommending that at least three stress levels are necessary although acknowledging that five might well be preferable.

To try to summarize the above rules and considerations, I have put together a hypothetical stress-performance graph as shown in viewgraph No. 3. The graph shows a range of accelerated testing and the anticipated deployment range. The accelerated range should be as wide as possible and is shown with five stress levels as discussed above. The same failure mode

will presumably be established on the basis of failure analysis of cells from the field and from accelerated testing. The straight line relationship shown is to indicate the continuity of failure from the accelerated into the deployment range. The fourth point on the viewgraph is the data base corresponding to the zero time cell population. Finally, lacking an obvious place to mark it on the graph, I have put a question mark referring to the possible effects of synergism or interaction between intentional and possibly unintentional stress situations.

Recalling some of my opening remarks about experiments on new materials and infant cells, there is obviously a subset of the above accelerated testing applying predominantly to materials and components. Results of investigations in this area are unlikely to be functional relations between stress situations and device lifetime. However, there will be very valuable data generated relating the effects of various stresses on new and developing materials. The remarks made above about the necessity for complete reporting and zero time data apply equally well in this area.

Deployment (Real-Time) Testing

Discussions in this area did not lead, or even show any promise of leading, to specified test procedures for real time or deployment testing. Substantial agreement was, however, reached in defining the manner in which such testing will be reported. The fourth viewgraph shows in summary the results of the discussions. Complete reporting of insolation conditions is well known to be extremely difficult, but a fair amount of information can be given so that other research groups can at least assess the reported results. Total insolation and peak insolation rates are reasonably easily measured and the requirement here would be to specify the measuring technique. Spectral content is an entirely different matter but as a minimum, the source of illumination should be specified. For example, AM1 simulation could be achieved with ELH lamps or with water filtered quartz-iodine. In the thermal area the important measurements would be the ambient temperature giving both the extrema and the average. There was at least one vigorous proponent of requiring that actual device temperatures also be reported. Other possibly important thermal data would be measurements of both time and spatial gradients of temperature. The experience with the flat-plate silicon arrays suggest that mechanical stresses may also play a prominent role in degradation. Ideally, one would like to know the residual stresses due to the thermal history of the device or array and also those stresses imposed due to thermal cycling, wind pressure and so on. The electrical loading of a cell or array obviously strongly influencesits lifetime and full information on the loading system should be given. Other ambient parameters which could influence cell life should be specified as appropriate.

This category could include information on humidity, wind, rain, dust and so on. Finallly on the viewgraph, although possibly it would have been more appropriate to put this first, would be complete information on the zero time data. This could inlcude the sample size, its manner of selection, and a complete description of the base or undegraded properties of the cells under test.

Other Subjects

In addition to the subjects covered above, there were various amounts of discussion on a number of other matters. These occurred at various times during the discussion period and I shall make no attempt to put them in any sort of logical order or rank them in order of priority.

The question was raised as to whether a central testing facility was either necessary or desirable. Those engaged in purely research activities could see no benefit to such a facility and felt that the turnaround time for information would be far too long. I don't wish to misquote the manufacturers who were represented, but my memory is that they felt other more conventional market forces would establish the credibility of a given product and so again there was little benefit in a central facility. One or two people could conceive of some value of such an activity to the sponsoring agencies who may be presented with the task of assessing and comparing the stability studies of different laboratories and organizations. A possible alternative that would serve most groups was seen as the establishment of a set of testing procedures which all parties would adhere to.

In the limited time, there were many topics not dealt with adequately or even in fact mentioned. I would suggest that a vital fact which we shall not be able to ignore is the high likelihood of synergism or interaction between various stressing systems. In due course, we will obviously have to take account of such interactions. Another area that received little if any attention was the precision with which accelerated testing would have to be conducted. If short term tests are to be used to project over long time periods, there are obviously some very rigorous requirements for the precision with which measurements are taken. A number of people drew attention to the fact that special research techniques will have to be developed for degradation studies. Finally, a subject which Dr. Feucht raised in one of the small meetings was that of using time shortening studies in contrast to actual accelerated testing. If the degradation mechanism is caused by the cycling of illumination rather than the total amount of illumination, then one could simulate a year's exposure in about a month by simulating very short days. There may well be a number of degradation modes which will fit in this category and considerable economy of testing time should be achievable.

I hope that the members of Group 1 feel that I have reasonably reported on their activities and not taken too many liberties to reduce many hours of discussion to a few minutes presentation.

John D. Meakin

Discussion Group II on Polycrystalline Si, MIS, and Conducting Oxide/Si Solar Cells and Materials

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I. Introduction

This workshop had seventeen members, with a balance of university (7), nonprofit and Government laboratories (6), and industry (4) participants. Because of the breadth of the topic and the immaturity of the technologies, it was impossible to arrive at any conclusions valid for all types of cells. We did, however, identify critical areas where more research is required.

II. Materials

A. Polycrystalline Si

There is a need for agreement on the definition of the term "polycrystalline silicon" since there are various classes, such as cast Si, CVD Si, and ribbon, each with greatly different properties.

The parameters pertinent to solar cells must be identified and measurement techniques established. It is important that for reporting the properties of polycrystalline Si, measurement standards exist to facilitate communication between workers. Examples of parameters might include resistivity, mobility, carrier lifetime, diffusion length, grain size and orientation, void space between grains, impurity content within the grains and at grain boundaries, etc.

B. Interfacial Layers

Guidelines should be developed for:

1. Thickness measurements of the interfacial layer. Since in some cells degradation has been associated with spontaneous growth of this layer, methods to measure its thickness with time should be developed.

2. Detection and characterization of pinholes.

3. Determination of the composition of the interfacial layer. This includes defects, impurities, and stoichiometry variations.

4. Determination of density and energy of charge states within the layer and at the silicon surface.

5. Identification of electronic transport mechanisms through the the interfacial layer.

C. Window Materials

By window, we mean the transparent metal used in MIS devices or the conducting oxide in the conducting oxide/Si cells.

It is important that the window materials do not react chemically with either the contact metal, the substrate, or the encapsulant. Properties of interest of the window material include its transmission spectrum, chemical stability, sheet resistance and resistivity, electronic properties (work function, electron affinity), and its mechanical integrity.

D. Contacts

Is electromigration a potential problem, especially in cells used with concentration?

III. Understanding and Characterization of Barriers

In *p-n* homojunction solar cells, the limitations of efficiency are well known and various parameters have been identified as relating to performance. Likewise, various figures of merit have been developed. In the devices discussed here, however, it is not clear what the relevant parameters are and what figures of merit are most meaningful.

IV. Potential Performance Goals

It is necessary to get a realistic prediction of the efficiencies attainable in each of the various material systems, as well as to identify the major problem areas. It is of little value to investigate the degradation mechanisms in those systems where it is known *a priori* that solar cells are impractical.

V. Potential Degradation Mechanisms

Clearly, all degradation mechanisms encountered in single crystal homojunction solar cells must be considered. In addition, processes related to the incompatibility of the various materials used (including those used for encapsulation) must be studied. The degradation mechanisms can be described as:

a. mechanical (e.g., crack propagation, strain induced by differences in thermal expansion),

b. interdiffusion of materials (including diffusion along grain boundaries),

c. chemical (e.g., oxidation),

d. electrochemical (resulting from internal as well as applied fields), and

e. photochemical.

Procedures for measurement of contact resistance and interfacial resistance (such as a four-point technique) are required so that the region of the degradation can be localized. Accepted techniques for measurement of interfacial charge as a function of stress (electrical, optical, thermal) should be developed.

VI. Guidelines and Standards for Measurements

Because of the great differences in the materials systems, it is not possible to develop measurement standards for degradation studies which are applicable to all cells. It is agreed, however, that initially procedures should be based on those for single crystal Si homojunction cells (being developed at Clemson University). In accelerated life tests, each investigator must make his own decision on deviating from these standards and, in reporting his results, must explain all such deviations.

As indicated earlier, standards must be established for characterization of polycrystalline Si.

Laboratory and deployment tests should be carried on simultaneously. Tests on nude cells should be made to determine the intrinsic degradation mechanisms. When necessary to isolate the cell from the ambient, they can be encapsulated.

VII. Recommendations for Further Research

Clearly, to understand degradation mechanisms, the principles of operations of the cells must be well understood.

A. We feel that more work must be done to determine the details of the principles of operation. An effort is required to correlate theory and experiment.

B. A greater effort is required to understand the pertinent properties of those materials which are candidates for solar cells. Why are different results obtained (consistently) in different laboratories? What parameters are affected by the different processing involved (e.g., is the work function of a window material really a function of its processing)?

C. More information is required concerning the thermodynamics, and particularly the kinetics, of reactions at interfaces in these cells.

D. A better understanding is needed concerning electrochemical reactions involving built-in as well as applied electric fields.

E. An effort is required to investigate interdiffusion of materials (interfacial layers, windows, grain boundaries, electromigration).

F. A knowledge is required of the mechanical and electrical properties of materials and cells as influenced by grain boundaries.

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Supplementary Report of the Discussion Group on Polycrystalline Si, MIS, and Conducting Oxide/Si Solar Cells and Materials

By

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Any discussion related to cell stability cannot ignore user needs in performance. You need also to talk about guidelines for defining and measuring this performance. This in turn leads inextricably to the need for developing performance standards or guidelines and test methods to demonstrate if devices developed can meet these performance standards. Both performance standards and test methods can and should be combined in one document.

There does not seem to be any way of ignoring the need to develop such a document of performance and test method standards if we are ever going to deal effectively with the problem of stability. Some NASA and other standards exist which may be adaptable to terrestrial solar cells. Others will need to be developed. My own personal feeling is that we need to have some kind of starting point, a document, even if imperfect, to provide a common ground of understanding. Improvements in such a document can develop in an evolutionary process as our knowledge about our solar cells becomes more sophisticated.

Among the questions that the working group discussed and which is an example of one of the issues that will need to be addressed in such a document is the following: should the different kinds of devices all meet the same set of guidelines or should they each, or by groups, have different ones to meet. That is, for example, should a MIS cell meet different performance standards than a *PN* homojunction?

In the vein of test methods and also of long life of solar cells, the topic of accelerated life testing was one of much concern to the members of the working group. There was concern about the high stress levels used in such tests triggering failure mechanisms that would not be a factor in affecting actual cell life. Such failure mechanisms would lead to bogus stability problems. Another source for bogus stability problems - one which could provide deceivingly optimistic life predictions - is to choose one variable to stress, leaving others nonstressed, and so ignore the situation where it is the combination of variables operating in concert that are important to long-term stability. The question of accelerated life testing is obviously very complicated and one where it will be difficult to agree how such tests should be performed and how the results of these tests should be interpreted.

Some in the working group felt that field tests should be initiated early so that they can be run in parallel with accelerated tests in the laboratory. Two different types of such tests can often produce significantly different results which can serve as an alert that more sophistication is needed.

Discussion Group III on Thin-Film GaAs

R. J. Stirn
Jet Propulsion Laboratory

Since GaAs thin-film solar cell technology is less mature than Si or Cu_2S/CdS technology, the recommendations of the Working Group (Table 1) are meant more to understand the mechanisms than to provide a means of predicting potential lifetimes of individual device structures independent of encapsulation.

Table 2 lists some degradation modes that may be present in GaAs thin-film structures. Under interdiffusion phenomena are several specific areas including degradation of high contact resistance between the GaAs and low cost substrate - especially over time at elevated temperatures, and in the case of AMOS-type GaAs cells, chemical reactions involving the barrier metal, interfacial oxide, and bulk GaAs such as out-diffusion of Ga, slow oxide growth, or oxide/metal, oxide/GaAs reactions which modify the interface state distribution such as discussed in an earlier paper. In the case of homojunction or heteroface solar cells, the ohmic front contact metallization is of concern, especially for concentration application. Either increasing contact resistance and/or delamination caused by water vapor exposure are potential problems. The use of indium tin oxide (ITO) or related materials as grid substitutes (not as a means of forming a heterojunction, which seems to be inherently poor in efficiency) may be a source of trouble due to chemical changes affecting the ITO light transmission or sheet resistance. Experience with ITO on Corning glass or sapphire substrates indicates no real stability problem, but that may not follow for ITO in contact with GaAs or with some Schottky barrier metal. The last category shown in Table 2 includes potential grain boundary diffusion, particularly in the case of a junction-type cell, where the diode characteristic may slowly deteriorate with time at somewhat elevated temperatures due to a low activation energy diffusion process.

A second major category of degradation mode is that of chemical effects, including those that are photo-enhanced or electrolytic in nature. The front contact corrosion problem and interfacial oxide modification in AMOS solar cells are obvious candidates, especially considering the fact that encapsulation cannot be expected to eliminate water vapor exposure completely.

A third major category includes degradation due to mechanical effects which may be very short term (catastrophic) or long term. The bonding between GaAs and the substrate should not be a problem if the bond has survived the initial high temperature and subsequent cool down during fabrication. Also, increasing series resistance of the Schottky barrier thin metal film with time due to rearrangement or conglomeration into island-like areas is not likely, unless a relatively high temperature is imposed. Normal

operating temperatures should be below the threshold where such a phenomena might occur. The most serious problem area for any solar cell structure is the rigidity of the front contacts and interconnects. Space qualified solar cells are required to undergo rather strenuous pull tests. Arrays for the low cost silicon project have not required pull test specifications as such on individual cells, since the encapsulation and module structure has an important influence on the overall reliability. Connections to a Schottky barrier-type cell is even more of a problem because of the need to contact to a thin metal film. A low temperature epoxy or solder contact will probably be required, at least for AMOS solar cells, with some kind of stress release mechanism for the interconnects.

With these various degradation modes in mind, the testing procedures were next discussed. The testing could be thought of as being both real-time and accelerated, with the former also acting as a screening technique to insure that relatively "robust" cells are examined for more extensive and demanding testing.

It is recommended that initial light and dark current-voltage characteristics and spectral response curves be taken in order to get a baseline characterization. Then the light and dark I-V characteristics should be measured over a range of temperatures - perhaps $-40^{o}C$ to $+50^{o}C$ in increments of $15^{o}C$. From these measurements, temperature coefficients of open-circuit voltage and other photovoltaic or diode parameters can be obtained.

Then to ensure having a "robust" cell, with which more demanding "accelerated" testing might be done, the cell should be cycled over this temperature range (in dry nitrogen) for about 50 cycles. If changes are observed after this cycling, the spectral response and I-V characteristics should be retaken for aiding in the determination of where the degradation is occurring.

Because of the many samples required and extensive data acquisition needed for even the few tests suggested here, only cells which have been fabricated using relatively major new processes should be selected. Certainly only representative cells from a fabrication scheme which has demonstrated reasonable reproducibility should be used.

For more severe testing, which may in some sense provide an "accelerated life testing", maintaining the test sample at an elevated temperature for a period of time is desirable. If enough temperature points are used, an Arrhenius plot can be made to determine activation energies if the degradation mode is thermally activated. The group suggested temperature points at 60, 90, 120, 150, 180, 240, and $300^{o}C$, assuming that the cells survive for a useful time, particularly within the higher range. Measurements should include the I-V characteristic in the dark and under illumination. For purposes of defining a common point of degradation for use on the Arrhenius plot, that point where the parameter such as maximum power, V_{oc} or I_{sc} is degraded to 75 percent of its original value could

be used. An atmosphere of dry nitrogen should be used. Clearly, the number of samples can get to be quite large and then the question of reproducibility in starting characteristics from one sample to the next is important. The degree of such testing will also be controlled by the resources made available to the investigator.

The recommended range of temperature and $30^{o}C$ increments were chosen so that it may be possible to determine if more than one degradation mechanism is present. This could show up as a break in the slope of the Arrhenius plot. Further complexity (and sample numbers) can also be added if test samples are separately loaded at short-circuit current or open-circuit voltage conditions.

Another test, much more severe in nature, would be to perform the above temperature versus time test, but under a humidified atmosphere. Should this be done, simply bubbling nitrogen through water at room temperature is recommended rather than trying to maintain some fixed relative humidity at each sample temperature.

The final topic of discussion within the GaAs Group was recommended research areas for thin-film GaAs and AMOS solar cells. Table 3 shows four general areas where it was felt that a more concentrated research effort would be most productive and meaningful for successful development of a viable solar cell. The first recommended subject - substrate selection and treatment - is the most crucial. Because of the very stringent economic goals for thin-film solar cells, steel and perhaps graphite substrates should be emphasized. Whether the GaAs is directly deposited on the substrate or whether an intermediate layer of recrystallized Ge is utilized, some passivating coating will be required to encourage larger grain growth, prevent alloying, provide good bonding and contact resistance, and for the case of a Ge layer, provide a surface which wets Ge. However, the latter requirement for Ge layers, and perhaps the alloying problem, may be sidestepped in that recrystallization may be limited only to the upper portion of the Ge film. This would greatly relax the requirements of the passivating coating. Possible candidates for the steel or graphite coatings are CVD coatings of tungsten, molybdenum, nitrides, or tungsten-carbide alloys.

As discussed in an earlier paper, degradation in the AMOS solar cell caused by chemical diffusion and/or electrolytic reactions are observed over long periods of time at elevated temperatures. However, the degradation rates do vary considerably for different types of interfacial oxides and for different barrier metals. Additional research in this area exploring the role of stoichiometry in oxides, deposited non-native oxides, and barrier metal alloys is required. X-ray photoelectron spectroscopy can play a major role in these studies.

The advantages of metal organic sources for large area deposition of GaAs with high gas utilization has been long recognized. Present-day quality control of purity and costs are unacceptable, however. A considerable

improvement in both purity and cost should automatically accrue when tank cars of TMG (trimethylgallium), for example, are required, rather than small numbers of laboratory stainless steel bottles. An alternative means of manufacturing TMG - perhaps prior to the extraction of ultra-high purity gallium from the ore sources - may be possible for further cost reduction. The degree of purity of TMG, arsine and hydrogen may be relaxed for GaAs thin-film solar cells, i.e., a "solar-grade" should be defined.

Finally, the metallization to GaAs and to Al(Ga)As needs to be improved using lower cost metals and, for thin-film structures, lower cost deposition techniques. Non-evaporative means for deposition of the grid contacts which do not lead to shorted junctions or degraded Schottky barriers, and yet provide good bonding and low contact resistance should be explored.

Table 1

ATTENDEES

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BENNER, JOHN	PLANNING RESEARCH CORP.
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CHU, SHIRLEY	SHOUTHERN METHODIST UNIV.
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OMAN, HENRY	BOEING COMPANY
SAHAI, RAJ	ROCKWELL SCIENCE CENTER
STIRN, RICHARD (LEADER)	JET PROPULSION LAB

*Part-time

Table 2

Degradation Modes

- Interdiffusion
  - GaAs/Substrate (contact resistance)
  - Metal/oxide/Ga
  - Front metallization (shallow homojunction, concentrator cell)
  - ITO when used as top electrode
  - Grain boundary
- Chemical, Photochemical, and Electrolytic
  - Front contact corrosion
  - Interfacial oxide growth and/or modification
- Mechanical
  - GaAs/substrate bonding
  - Semitransparent Metal Film (sheet resistance)
  - Front contact integrity (AMOS and junction)

Table 3

Recommended Areas of Research

- Substrate Selection and Treatment
- Degradation Mechanisms of AMOS
- TMG, TMA, Arsine Quality
- GaAs and Al(Ga)As Metallization

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16. ABSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)*

A workshop was held to discuss what needs to be done to achieve and measure long term stability of terrestrial solar cells using thin film materials and device technologies. Under this theme, researchers in the field and invited speakers from related device technologies presented papers and took part in discussions related to solar cells of the following three material groupings: (1) Cu_2S/[CdZn]S, Cu-ternaries/CdS, InP/CdS, and amorphous Si; (2) polycrystalline, metal-insulator-semiconductor (MIS), and conducting-oxide Si; and (3) polycrystalline and antireflection-coated metal-oxide-semiconductor (AMOS) GaAs. This workshop report contains the 18 papers presented and the reports of three discussion groups; it also includes a section on the highlights of these papers and reports. The many needs identified by the workshop participants can be organized into two general areas of work to be done. One area of work is in the development of an improved understanding of cell operation and of component structures of these cells. The other is in the development of an improved measurements base.

17. KEY WORDS *(six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons)*

Accelerated tests; failure mechanisms; failure modes; photovoltaics; reliability; semiconductors; solar cells; stability; testing; thin films.

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